Thin Solid Films 573 (2014) 18–21

Contents lists available at ScienceDirect

Thin Solid Films

journal homepage: www.elsevier.com/locate/tsf

Temperature dependence of the electrical characteristics of low-temperature processed zinc oxide thin film transistors

M. Estrada [a,*], G. Gutierrez-Heredia [d], A. Cerdeira [a], J. Alvarado [b], I. Garduño [b], J. Tinoco [c], I. Mejia [d], M. Quevedo-Lopez [d]

[a] SEES, Depto. de Ingeniería Eléctrica, CINVESTAV-IPN, Av. IPN 2208, CP 07360 México DF, México
[b] CIDS, Instituto de Ciencias, Benemérita Universidad Autónoma de Puebla, CP 72570 Puebla, México
[c] Micro and Nanotechnology Research Centre (MICRONA), Universidad Veracruzana, Av. Ruíz-Cortinez 455, CP. 94294 Boca del Rio, Veracruz, México
[d] Materials Science and Engineering Department, University of Texas at Dallas, Richardson, TX 75080, USA

ARTICLE INFO

Article history:
Received 21 December 2013
Received in revised form 23 October 2014
Accepted 29 October 2014
Available online 5 November 2014

Keywords:
Zinc oxide
Thin film transistors
Temperature
Low-temperature processing
Pulse laser deposition

ABSTRACT

The impact on the electrical behavior of thin film transistors, TFTs, based on zinc oxide, ZnO-based TFTs, with temperature is analyzed. ZnO is deposited using pulsed laser deposition techniques and the temperature used during the entire fabrication process is kept below 100 °C. Up to 330 K, the transfer curves practically remain constant or slightly shifted toward more positive voltages. For temperatures up to 330 K, they show the combined effect of the threshold voltage shifting toward more negative voltages and the increase of series resistance. The drain current shows an Arrhenius-type dependence with temperature in subthreshold regime with activation energy of around 0.53 eV. In above threshold regime, for temperatures above 330 K, the activation energy is around 0.15 eV.

1. Introduction

Oxide semiconductor thin film transistors, OSTFTs, have made an impressive progress particularly in display applications in a relatively short time [1]. Among the advantages of these devices are their high optical transparency [2,3], a relatively high electron mobility [4], as well as the possibility of using low temperature and relatively low cost processing techniques [1,3].

Although initial attempts of using zinc oxide, ZnO, as active layer appeared during the 60s [5], the birth of transparent electronics is normally associated with ZnO TFTs presented in 2003, when transparent conductive oxide based electrodes and mobility as high as 2.5 $cm^2 V^{-1} s^{-1}$, were reported [2]. However, some of these approaches utilize high post-processing temperatures incompatible with emerging low-temperature flexible electronics [6,7]. Not to mention, some of them use very crude patterning techniques (e. g. shadow mask or common back gate contact), which prohibit the implementation and optimization of high performance circuits [2,8]. An important step in advance was the development of fabrication techniques, using low or even room temperature processes [1,3,8].

Regarding the electrical characteristics of OSTFTs, much interest has been dedicated to increase mobility, as well as the stability of the devices. To increase stability, amorphous multi-component oxide layers containing indium–gallium–zinc oxides, IGZO, or hafnium–indium–zinc oxides, HIZO, have been studied [1,9]. The temperature, *T*, behavior of the electrical characteristics, however, has not been sufficiently studied. Some articles presenting the behavior of OSTFTs with temperature can be found, but usually, they cover temperatures below 300 K [10–12].

In this work we analyze the behavior in the temperature range of 300 K to 370 K, of the electrical characteristics of ZnO TFTs fabricated with temperature processes not exciding 100 °C. Possible causes for the observed effects are discussed.

2. Experimental part

ZnO TFTs with the bottom-gate top-contact configuration shown in Fig. 1a were fabricated as reported in [3]. The process consists of 100 nm of patterned gold film to serve as a gate metal. The hafnium oxide, HfO_2, dielectric layer is deposited by atomic layer deposition at 100 °C and patterned with a buffered oxide etch solution. The ZnO layer is deposited by pulsed laser deposition and subsequently covered by 500-nm of poly-p-xylylene-C (Parylene-C) deposited by chemical vapor deposition at room temperature, which is used as a protective/hard-mask film. Source and drain vias are opened through the hard-mask film using reactive ion etch. The next step is to deposit 100 nm of aluminum layer that will serve, after a photolithographic process, as the source and drain contacts. Fig. 1b shows an optical micrograph of

* Corresponding author.
E-mail address: mestrada@cinvestav.mx (M. Estrada).

http://dx.doi.org/10.1016/j.tsf.2014.10.092
0040-6090/

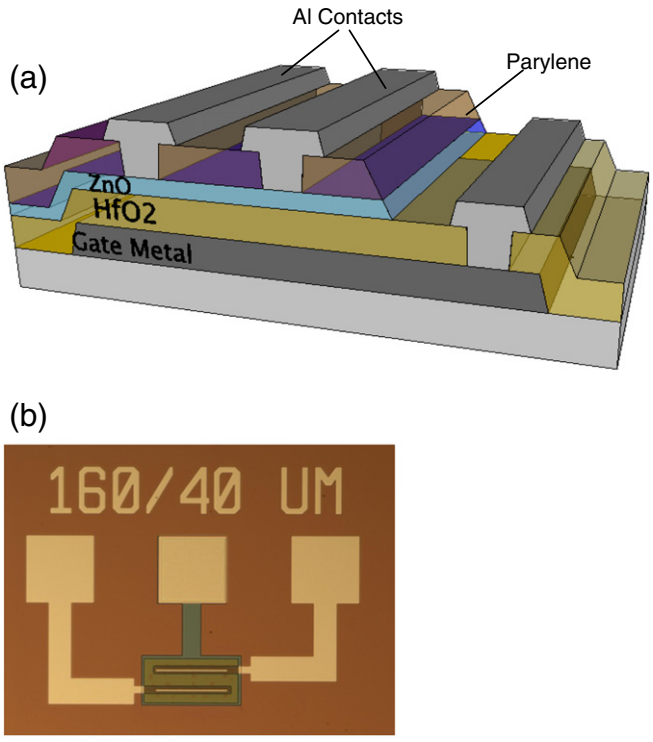

Fig. 1. a) Cross section of the analyzed ZnO TFT; b) optical micrograph of a TFT.

an actual TFT. TFTs with different channel widths ($W = 40$, 80 and 160 μm) and channel lengths ($L = 20$, 40 and 80 μm) are included in each die.

Electrical measurements at different temperatures were done in dark and in vacuum conditions, using a K20 programmable temperature controller and measurement chamber from MMR Technologies Inc. and a Keithley 4200 semiconductor characterization system.

The linear transfer curves and transfer curves in saturation, as well as the output characteristics for devices with different W/L ratios were measured in the temperature range between 300 K and 370 K, making sure that the variation of the drain current, I_{DS}, was due to the temperature variation and not to instability effects. Since the characteristics for all devices showed a similar behavior, results will be analyzed for a device with $W = 160$ μm and $L = 40$ μm.

3. Analysis and discussion of results

Analyzing the electrical characteristics of the fabricated TFTs, it was observed that during the first measurements at room temperature, the devices presented threshold voltage, V_T, instability. For this reason, measurements with temperature were done after several consecutive measurements, until the devices were stabilized and measurements at room temperature repeated.

Fig. 2a and b shows the linear transfer characteristics measured in the temperature range between 300 and 370 K. It is seen that, as the temperature is increased up to around 330 K, the transfer curves practically remain constant or shift slightly toward more positive voltages, see Fig. 2a. As the temperature is further increased, the curves shift toward negative voltages. At the same time, up to $T = 340$ K and for gate voltages, V_{GS}, greater than 5 V, an increase of the channel and series resistance, R_S, is observed, represented by the decrease of the drain current, I_{DS}, as the temperature is increased. For higher temperatures, the maximum value of I_{DS} tends to saturate and the gate voltage at which this saturation appears is reduced.

In Fig. 2b, the same curves are plotted in a semilog scale to see in more detail the V_T shift with temperature. In Fig. 3, a similar behavior of V_T is observed for the transfer curve in saturation, although the shift to the left is smaller.

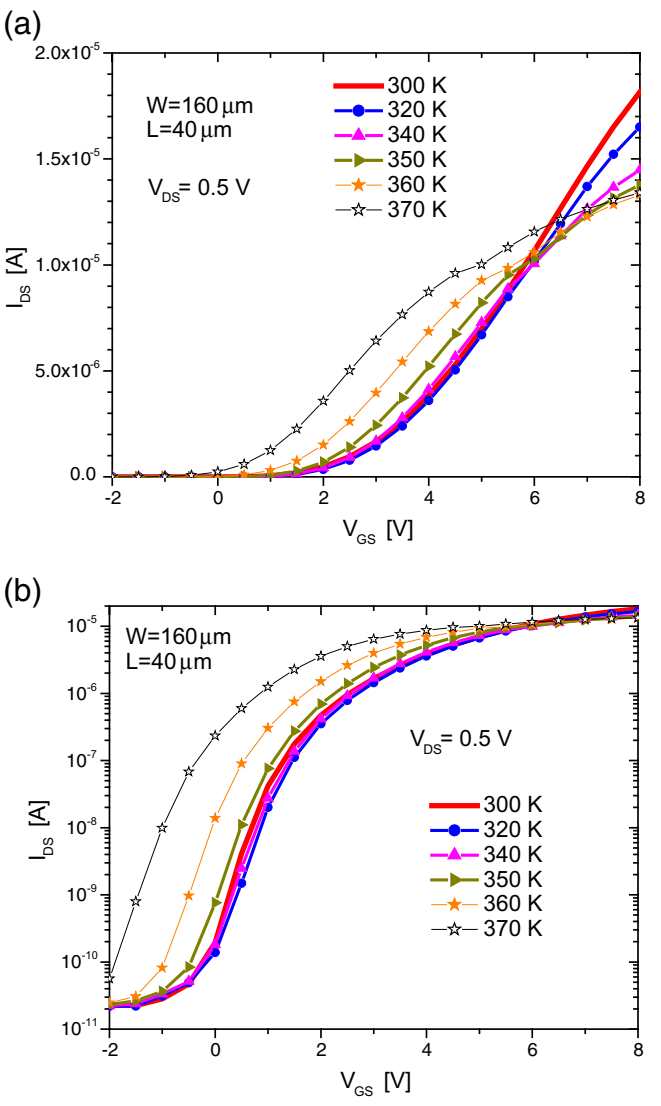

Fig. 2. Linear transfer characteristic at $V_{DS} = 0.5$ V in the temperature range from 300 K to 370 K: a) natural plot; b) semilog plot.

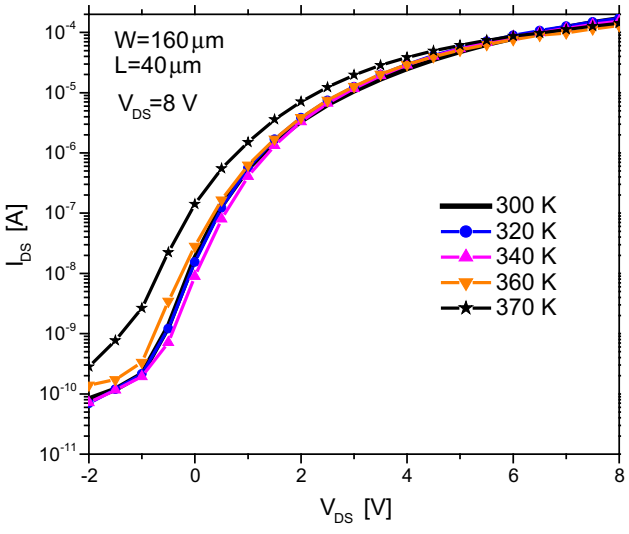

Fig. 3. Saturation transfer characteristic at $V_{DS} = 8$ V in the temperature range from 300 K to 370 K in semilog plot.

The two effects observed up to now are the reduction of V_T and the increase of R_S with temperature. Both effects have been observed previously for oxide semiconductor materials. The reduction of V_T with increasing temperature has been reported previously for IGZO TFTs [13], where authors showed by simulation, that the effect can be explained by the presence of a high concentration of shallow traps near the conduction band of the active layer.

The presence of a positive temperature coefficient for the resistivity, that can explain the increase in R_S with temperature observed for analyzed devices, has been observed before for ZnO layers [14]. In the referred work, using previously reported data for ZnO shallow donor-like states ionization energy and Fermi level, authors demonstrated that the combined effect of free-carrier density approaching saturation and reported mobility behavior for these layers [15] can produce a positive temperature coefficient for the layer resistivity.

The typical behavior of the output characteristics with temperature is shown in Fig. 4. For gate voltages, $V_{GS} = 2$ V and 5 V, it is observed that the drain current increases with temperature due to the reduction of the V_T already mentioned. For $V_{GS} = 8$ V, an interesting effect is observed, resulting from the combined effect of increasing R_S with temperature and reducing the threshold voltage. It is seen that in the linear region, I_{DS} decreases and the on resistance, R_{on}, increases as T is increased, indicating the increase of R_S, with T. Also, as the drain voltage, V_{DS}, is increased, the drain current first decreases for temperatures between 300 K and 340 K, starting to increase again for $T > 340$ K. For this last case, I_{DS} in the output curves does not show a clear saturation with V_{DS}, as observed for $T < 340$ K. At a certain sufficiently high value of V_{DS}, I_{DS} becomes even higher than the one corresponding to $T = 300$ K. The same trend is observed for the curve corresponding to $T = 360$ K, where I_{DS} is expected to become higher than its value for $T = 300$ K at a value of V_{DS} greater than 8 V, which is the maximum value at which the device was measured. The explanation of this behavior will be discussed below.

Figs. 5 and 6 show the variation of the drain current as a function of $1000/T$ in the subthreshold and above threshold regimes, respectively. In subthreshold regime, the drain current increases with temperature, showing Arrhenius-type dependence with activation energy of around 0.53 eV.

In Fig. 6a, for above-threshold regime, the Arrhenius-type dependence has two slopes. The first one, is observed for T > 330 K and the activation energy, when $V_{DS} > V_{GS}$, is around 0.15 eV. For T < 330 K, the slope is much smaller, but I_{DS} also increases as T increases."

If $V_{DS} \leq V_{GS}$ and $T > 330$ K the Arrhenius-type dependence is no longer evident and I_{DS} can even increase as T decreases, as shown in Fig. 6b.

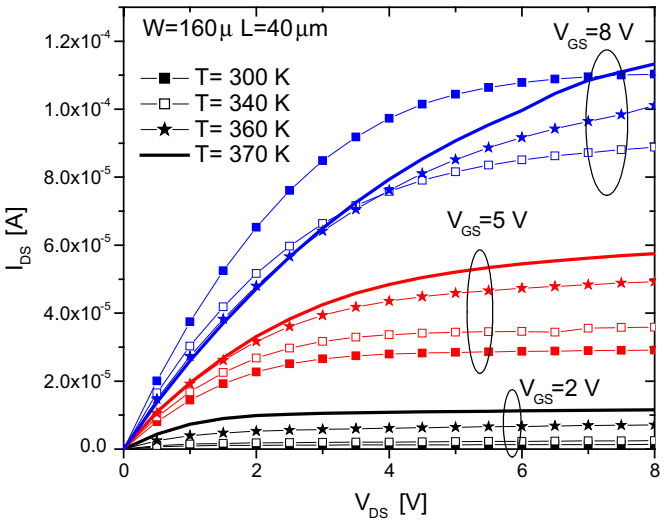

Fig. 4. Output characteristics in the temperature range from 300 K to 370 K.

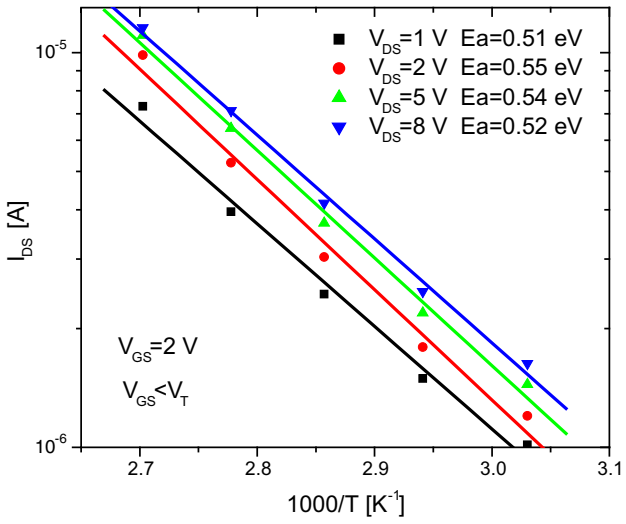

Fig. 5. Temperature dependence between 300 K and 370 K of I_{DS} in subthreshold regime.

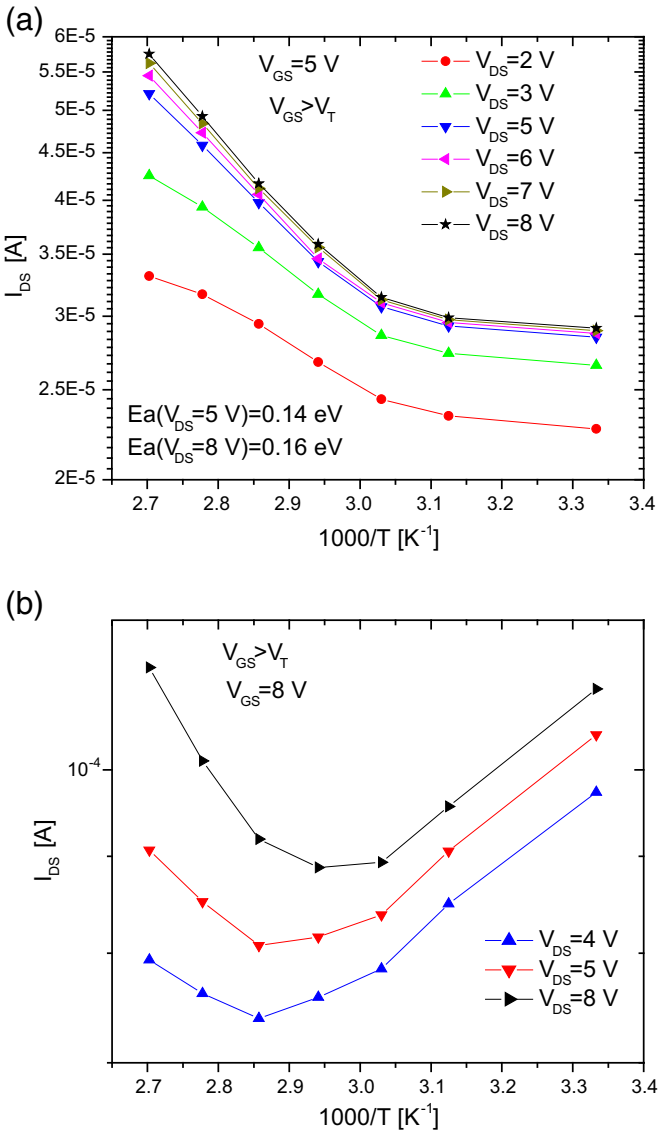

Fig. 6. Temperature dependence between 300 K and 370 K of I_{DS} in above threshold for a) $V_{GS} = 5$ V and b) $V_{GS} = 8$ V.

The increase of I_{DS} in terms of $1/T$ observed in Fig. 6b in the above threshold regime for T <350 K can also be explained by the effect of R_S already mentioned, since carriers must move from the drain across the ZnO layer to reach the channel.

To further support that the behavior of I_{DS} vs. V_{DS} for $V_{GS} = 8$ V is explained by the combined effect of the reduction of V_T and the increase of R_S, in Fig. 7 we compare a modeled curve considering these two effects, with measured curves. Device parameters used for modeling were extracted from measurements and are shown in Table 1. V_T was calculated by the second derivative method [16]. Using these parameters, the drain current was calculated as [17]:

$$I_{DS} = \frac{K \cdot \mu_{FET}}{[1 + R \cdot \mu_{FET} \cdot (V_{GS} - V_T)]} \cdot \frac{(V_{GS} - V_T) \cdot V_{DS} \cdot (1 + \lambda \cdot V_{DS})}{\left[1 + \left[\frac{V_{DS}}{\alpha_s (V_{GS} - V_T)}\right]^m\right]^{1/m}} \quad (1)$$

where $K = \frac{W}{L} C_i$; C_i is the capacitance per unit area and W and L are the channel width and length, respectively. The relative dielectric constant used for the HfO_2 was 14.

Fig. 7 shows the measured and modeled output characteristics for $V_{GS} = 8$ V for temperatures of 300 K, 340 K and 370 K. It is seen that both the measured and modeled I_{DS} reduce with temperature, being smaller at 340 K than for 300 K. As the temperature is further increased the values of I_{DS} can become higher than those corresponding to a lower temperature. In Fig. 7, it is seen that the drain current for both the measured and modeled curves at 370 K can reach values above those observed for 340 K. These results confirm that considering the combine effect of the R_S increase and the V_T shift when modeling the output characteristics of the analyzed TFT, the experimental behavior of I_{DS} with temperature can be well reproduced. The increase of R_{on} is also reproduced. These results also confirm the importance of achieving low values of R_S in the fabricated devices.

4. Conclusions

The behavior with temperature of the electrical characteristics of ZnO TFTs, fabricated with low temperature processes (T < 100 °C) is analyzed. It is seen that up to 330 K, the transfer curves practically remain constant or displace slightly toward more positive voltages. At temperatures above 330 K, the combined effect of the reduction of V_T and the increase of R_S tends to saturate the current in the transfer characteristics. The drain current shows an Arrhenius-type dependence with temperature in subthreshold regime with activation energy of around 0.53 eV. In above threshold regime, for T >330 K and $V_{DS} > V_{GS}$, the activation energy is around 0.15 eV. If $V_{DS} \leq V_{GS}$ and T > 330 K, the I_{DS} no longer follows an Arrhenius-type dependence and decreases as T increases, which can be explained by an increase with T of R_S associated to the active layer that the carriers have to cross, when moving between top drain and source contacts and the channel.

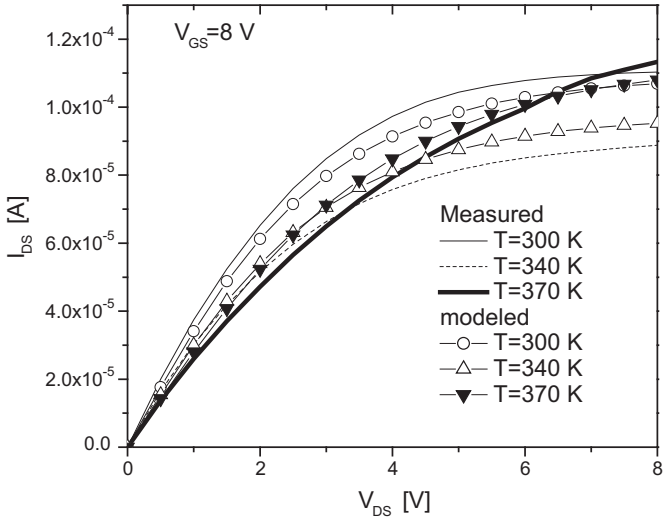

Fig. 7. Measured and modeled output characteristic for $V_{GS} = 8$ V at temperatures between 300 K and 370 K. The modeled curve considers the combined effect of series resistance increase and V_T shift as temperature increases.

Table 1
Extracted device parameters.

T [K]	V_T [V]	R [Ω]
300	3.5	556
310	3.5	883
320	3.5	1480
330	3	2600
340	3	5000
350	2.5	8400
360	2	11,800
370	1	15,000

Acknowledgements

This work was supported by CONACyT project 127978 in Mexico, VIEP and PROMEP DSA/103.5/14/projects of BUAP, CONACyT interchange programs and the National Science Foundation (NSF).

References

[1] E. Fortunato, P. Barquinha, R. Martins, Oxide semiconductor thin-film transistors: a review of recent advances, Adv. Mater. 24 (2012) 2945.
[2] R.L. Hoffman, B.J. Norris, J.F. Wager, ZnO-based transparent thin-film transistors, Appl. Phys. Lett. 82 (2003) 733.
[3] G. Gutierrez-Heredia, I. Mejia, M.E. Rivas-Aguilar, N. Hernandez-Como, V.H. Martinez-Landeros, F.S. Aguirre-Tostado, M.A. Quevedo-Lopez, Fully patterned and low temperature transparent ZnO-based inverters, Thin Solid Films 545 (2013) 458.
[4] S.J. Pearton, C.R. Abernathy, M.E. Overberg, G.T. Thaler, D.P. Norton, N. Theodoropoulou, A.F. Hebard, Y.D. Park, F. Ren, J. Kim, L.A. Boatner, Wide band gap ferromagnetic semiconductors and oxides, J. Appl. Phys. 93 (1) (2003) 1.
[5] G.F. Boesen, J.E. Jacobs, ZnO field-effect transistor, Proc. Inst. Electr. Electron. Eng. 56 (11) (1968) 2094.
[6] J. Nishii, F.M. Hossain, S. Takagi, T. Aita, K. Saikusa, Y. Ohmaki, I. Ohkubo, S. Kishimoto, A. Ohtomo, T. Fukumura, F. Matsukura, Y. Ohno, H. Koinuma, H. Ohno, M. Kawasaki, High mobility thin film transistors with transparent ZnO channels, Jpn. J. Appl. Phys. 42 (2003) L347.
[7] B.J. Norris, J. Anderson, J.F. Wager, D.A. Keszler, Spin-coated zinc oxide transparent transistors, J. Phys. D Appl. Phys. 36 (2003) L105.
[8] E.M.C. Fortunato, P.M.C. Barquinha, A.C.M.B.G. Pimentel, A.M.F. Goncalves, A.J.S. Marques, L.M.N. Pereira, R.F.P. Martins, Fully transparent ZnO thin-film transistor produced at room temperature, Adv. Mat. 17 (2005) 590.
[9] S.-Y. Sung, J.H. Choi, U.B. Han, K.C. Lee, J.-H. Lee, J.-J. Kim, W. Lim, S.J. Pearton, D.P. Norton, Y.-W. Heo, Effects of ambient atmosphere on the transfer characteristics and gate-bias stress stability of amorphous indium–gallium–zinc oxide thin-film transistors, Appl. Phys. Lett. 96 (2010) 102107.
[10] X. Huang, C. Wu, H. Lu, F. Ren, D. Chen, R. Jiang, R. Zhang, Y. Zheng, Q. Xu, Temperature and gate bias dependence of carrier transport mechanisms in amorphous indium–gallium–zinc oxide thin film transistors, Solid-State Electron. 86 (2013) 41.
[11] E. Chong, K.-H. Park, E.A. Cho, J.Y. Choi, B. Kim, D.-Y. You, G.-E. Jang, S.Y. Lee, Correlation between the stability and trap parameters of amorphous oxide thin film transistors, Microelectron. Eng. 91 (2012) 50.
[12] K. Hoshino, J.F. Wager, Operating temperature trends in amorphous In–Ga–Zn–O thin-film transistors, IEEE Electron. Device Lett. 31 (8) (2010) 818.
[13] H. Godo, D. Kawae, S. Yoshitomi, T. Sasaki, S. Ito, H. Ohara, H. Kishida, M. Takahashi, A. Miyanaga, S. Yamazaki, Temperature dependence of transistor characteristics and electronic structure for amorphous In–Ga–Zn-Oxide thin film transistor, Jpn. J. Appl. Phys. 49 (2010) 03CB04.
[14] D. Fernández-Hevia, J. de Frutos, A.C. Caballero, J.F. Fernández, Bulk-grain resistivity and positive temperature coefficient of ZnO-based varistors, Appl. Phys. Lett. 82 (2003) 212.
[15] Ü. Özgür, Y.I. Alivov, C. Liu, A. Teke, M.A. Reshchikov, S. Doan, V. Avrutin, S.-J. Cho, H. Morkoç, A comprehensive review of ZnO materials and devices, J. Appl. Phys. 98 (2005) 041301.
[16] A. Ortiz-Conde, F.J.G. Sanchez, J.J. Liou, A. Cerdeira, M. Estrada, Y. Yue, A review of recent MOSFET threshold voltage extraction methods, Microelectron. Reliab. 42 (2002) 583.
[17] T.A. Fjeldly, T. Ytterdal, M. Shur, Introduction To Device Modeling and Circuit Simulation, John Wiley and Sons, Inc, USA, 1998.