Compact model for short-channel symmetric double-gate junctionless transistors

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ABSTRACT

In this work a compact analytical model for short-channel double-gate junctionless transistor is presented, considering variable mobility and the main short-channel effects as threshold voltage roll-off, series resistance, drain saturation voltage, channel shortening and saturation velocity. The threshold voltage shift and subthreshold slope variation is determined through the minimum value of the potential in the channel. Only eight model parameters are used. The model is physically-based, considers the total charge in the Si layer and the operating conditions in both depletion and accumulation. Model is validated by 2D simulations in ATLAS for channel lengths from 25 nm to 500 nm and for doping concentrations of $5 \times 10^{18}$ and $1 \times 10^{19}$ cm$^{-3}$, as well as for Si layer thickness of 10 and 15 nm, in order to guarantee normally-off operation of the transistors. The model provides an accurate continuous description of the transistor behavior in all operating regions.

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1. Introduction

Junctionless transistors (JLT) [1] are one of the most promising MOSFET devices for the continuity of downscaling, consisting in a silicon nanowire with same type of doping concentration from source to drain. These nanowire transistors, proposed in 2009 [1], can be fabricated in a similar way as FinFET transistors, but with the same doping type material from source to drain and with/without additional doping concentration in the extensions.

Heavily doped silicon layer is used to increase the device conductivity whereas the silicon thickness has to be thin enough, in order to allow full depletion of the layer and current cut-off. Transistors can be considered as double-gate or tri-gate MOSFETs [2–6] and the scaling properties are analyzed in [7,8].

The first step in the analysis of JLTs is to consider a double-gate junctionless transistor (DGLT), which can be done in two ways: 1) considering a 3D structure where the top gate in the tri-gate has a thick dielectric and no influence in the current conduction; 2) using a typical double-gate structure with long channel width as the structure shown in Fig. 1.

Different analyses of performance and possible applications of these devices are presented in [9–12].

A good model for current–voltage characteristics is always required for the application of these devices, reason why different papers have presented approximate numerical–analytical and analytical models for specific regions of operation [13–16] and for all regions [17–23]. The study of short channel effects in JLT with no homogeneous doping profile has been performed firstly in [24] for subthreshold regime and in [23] another model was presented for all regimes, both models with additional source and drain implantations with the aim of reducing the series resistance and improving the subthreshold slope.

In all these papers, different approximations are considered for mobile charges in the depletion and accumulation regions, obtaining approximate I–V characteristics. In [18] the channel with one part in depletion and another in accumulation was defined and calculated as hybrid channel. The main problem for DGLT modeling is the transition from the depletion mode of operation to the accumulation mode, because the physical behavior in both regions is different. For DGLTs in deep depletion, below threshold voltage and in depletion below flat-band voltage, the current is defined by the charge transport at or near the center of the silicon layer (also referred as body current). For gate voltages larger than the flat-band voltage, $V_{FB}$, accumulation is reached and the current flows along the whole silicon layer, although the surface current at both interfaces is predominant.

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Recently we presented a DGJLT model for long channel transistors considering the total mobile charge in the silicon layer, from center to the surface and the series resistance using numerical calculations [25]. Afterward, for the same structure, an analytical model was published [26].

The introduction of short-channel effects using numerical modeling was presented in [27,28]. In this work an analytical model for short-channel DGJLT is presented, considering the main short-channel effects such as the increase of the body potential due to drain bias, mobility degradation due to vertical and horizontal electric fields and carrier velocity saturation. The source and drain silicon extensions are considered with 30 nm length and highly doped, in order to obtain better performance in analytical applications [29] and to increase the current with the same high doping concentration and silicon layer thickness.

2. Model description

2.1. Potentials

The analyzed DGJLT structure is shown in Fig. 1, where $L$ is the channel length; $W$ is the channel width; $t_{ox}$ is the equivalent oxide thickness (EOT); $t_s$ is the silicon layer width and $L_{ext}$ are the silicon extensions at drain and source. $N_0$ is the doping concentration below the gate and $N_{Dext}$ is the doping concentration in the extensions. Majority carriers are present inside the whole silicon layer, which is considered the transistor channel. The difference of potential in the silicon layer between the surface, $\varphi_s$, and the center, $\varphi_c$, normalized to thermal potential, $\varphi_t$, can be calculated using the following expression, [26]:

$$\alpha = \alpha_{st} + LW \left[ -\alpha_{st} e^{-\alpha_{st} x} e^{-\alpha_{st} y} \right].$$

where $\alpha_{st}$ is the normalized difference of potentials in deep subthreshold, $V$ the voltage drop along the channel and $LW$ is the Lambert function implemented using the Halley's method, which has been successfully used in all our previous models [31,32].

The relation between the surface potential and the applied gate and drain voltages, $V_G$ and $V_D$, is given by:

$$V_G - V_{FB} = \varphi_s + \text{sign}(x) \varphi_f \sqrt{\frac{\alpha_{st} y}{e^{\alpha_{st} y} - \xi \cdot x - 1}},$$

where $\alpha_{st}$ is the silicon dielectric constant, $\varepsilon_{ox}$ is the SiO$_2$ dielectric constant; gate capacitance per unit of area is equal to $C_{ox} = \varepsilon_{ox} / t_{ox}$; the silicon layer capacitance per unit of area is equal to $C_s = \varepsilon_s / t_s$; $\gamma = C_0 (4C_s)$; $q_d$ is the total normalized fixed charge in the silicon layer; $q$ is the charge of the electron.

There is no an exact analytic answer to solve (2), the potentials can only be obtained with numerical analysis. In this model a solution of (2) is obtained applying an iterative method with cubically convergence, the equation is solved with maximum two iterations obtaining a precision better than 0.01%.

A detailed description of the solution method can be finding in Appendix A.

2.2. Charges

Taking into account the symmetry of the double-gate device, one half of the channel is studied, the total mobile charge from the surface to the center of the Si layer, is equal to:

$$q_m = -\text{sign}(x) \beta \sqrt{\frac{e^{\alpha_{st} y} - x \cdot \xi - 1}{\varphi_t}} q_d.$$

Drain current is calculated by integrating (3). However, this cannot be performed in one step, making necessary to decouple the charge for the different regimes of operation: depletion and accumulation, each depending only of one variable, as was done in [26]. Within the depletion region, the total charge is expressed as a function of de variable $x$, as follows:

$$q_{dep} = \beta \sqrt{e^{\alpha_{st} y} - \xi \cdot x - 1}.$$

Whereas in the accumulation region, the total charge is a function of $\varphi_s$ expressed as:

$$q_{acc} = -\beta \sqrt{e^{-\alpha_{st} y} - \frac{\varphi_s - V}{\varphi_t} - 1}.$$

To describe the charge through a continuous expression it is needed to capture the transition in a smooth function. As successfully applied in previous models [31,32] the transition between depletion to accumulation is obtained using tanh function, guaranteeing continuity of the function and its derivatives. The single-piece continuous equation of the total charge is:

$$q_{tst} = q_{dep} \left[ 1 - \tanh(25[V_G - (V_F B + V_D)]) \right] + q_{acc} \times \frac{1}{2} \left[ 1 + \tanh(25[V_G - (V_F B + V_D)]) \right].$$

2.3. Threshold voltage

An accurate definition of the threshold voltage for long channel JLT, $V_{th}$, was derived in [25], using the following expression:

$$V_{th} = V_{FB} - \varphi_f \left[ \frac{q_d}{2} - \frac{1}{4} - x_T - \ln \left( 1 - \frac{x_T}{\alpha_{st}} \right) \right],$$

where the normalized difference of potentials at the threshold voltage is equal to:

$$x_T = \frac{\alpha_{st} \left[ 1 - \alpha_{st} \left( 1 - \frac{1}{2q_d} \right)^2 \right]}{1 - \alpha_{st} \left( 1 - \frac{1}{2q_d} \right)^2}.$$
\( V_{\text{Dsat}} = V_C - V_{T0} \). 

After a detailed analysis using numerical simulations, for \( L < 300 \) nm, the effect of the saturation velocity \( u_{sat} \) on the drain saturation voltage when the channel length is reduced can be expressed by:

\[
V_{\text{Dsat}} = 0.08 + \eta (LV_{\text{sat}})^{0.33} (V_C - V_{T0}),
\]

where \( \eta \) is an adjusting parameter.

The final value of \( V_{\text{Dsat}} \) is taken as the smaller of the two values obtained from (9) and (10). The effective drain voltage \( V_{\text{Deff}} \) is defined through \( V_{\text{Dsat}} \) as:

\[
V_{\text{Deff}} = V_{\text{Dsat}} + \frac{1}{2} \left[ V_D - V_{\text{Dsat}} + \varphi_1 - \sqrt{(V_D - V_{\text{Dsat}} + \varphi_1)^2 + 4\varphi_1 V_{\text{Dsat}}} \right].
\]

### 2.5. Channel shortening

When the drain voltage is greater than the saturation voltage, \( V_D > V_{\text{Dsat}} \), the depleted region moves toward the source, reducing the effective channel length \( L_{\text{eff}} = L - \Delta L \). This reduction is calculated through the following expression:

\[
\Delta L = \lambda \sqrt{\frac{2e_k}{qN_D} (V_D - V_{\text{Ddef}})},
\]

where \( \lambda \) is an adjusting parameter. When \( V_D < V_{\text{Dsat}} \), \( \Delta L = 0 \).

### 2.6. Subthreshold characteristic

In subthreshold regime, the 2D channel electrostatic potential for an N-type silicon layer with doping concentration \( N_D \) and the structure presented in Fig. 1, is calculated solving Poisson’s equation, considering that the total charge is approximately equal to the fix charge (full depletion):

\[
d^2 \varphi(x,y) \over dx^2 + d^2 \varphi(x,y) \over dy^2 = - \frac{q N_D}{\varepsilon_S},
\]

where \( \varphi(x,y) \) is the 2-D potential distribution below the channel.

Considering a parabolic approximation for the potential distribution in the x-direction as suggested by Young [34]:

\[
\varphi(x,y) = A(y) \cdot x + B(y) \cdot x + C(y),
\]

the coefficients \( A, B \) and \( C \) are determined by applying in (14) the Gauss boundary conditions for the electric field at the surface and at the center of the Si layer:

\[
\varphi(x,y) \bigg|_{x=-t_S/2} = \frac{V_C - V_{T0} - \varphi_3(y)}{t_{ox}} \frac{t_{ox}}{\varepsilon_S},
\]

\[
\varphi(x,y) \bigg|_{x=0} = 0,
\]

a relation for the potential as a function of the potential at the plane center, \( \varphi(0,y) = \varphi_0(y) \), is achieved through:

\[
\varphi(x,y) = \varphi_0(y) + \frac{4y^2}{t_S^2} \left( \frac{V_C - V_{T0}}{t_{ox}} - \frac{1}{1 + \gamma} \left| \varphi_0(y) + (V_C - V_{T0}) \gamma \right| \right) x^2.
\]

Substituting (17) in (13) and solving the resulting differential equation, we obtained the potential at \( x = 0 \). The minimum value of this potential, \( \varphi_{\text{min}} \), can be obtained from:

\[
\varphi_{\text{min}} = \sqrt{(U_S^2 + U_D^2) + 2U_S U_D \cosh(L/t_n)} + \varphi_{\text{Sr}}.
\]

where \( U_S = V_{VSS} - \varphi_{\text{Sr}}, U_D = V_{SS} - \varphi_0(y), t_n \) is the double-gate natural length [33] and \( \varphi_{\text{Sr}} \) is the subthreshold potential at the center of the Si layer for a long channel device, which is equal to:

\[
\varphi_{\text{Sr}} = V_C - V_{T0} + \frac{qN_{D0}}{\varepsilon_S} t_n^2.
\]

and \( V_{VSS}, V_{SS} \) are the built-in potential at source and drain respectively.

A built-in effective voltage is calculated to take into account the effect of the \( S \) and \( D \) extensions on \( V_{\text{th}} \) which is calculated as proposed in [23]:

\[
V_{\text{th},S,D} = \varphi_{\text{Sr}} - \frac{qN_{D0} t_n^2}{\varepsilon_S} \left( 1 - \sqrt{1 + \frac{4}{q} \left( V_{VSS} + V_{SS} - \varphi_{\text{Sr}} \right) t_n^2} \right). \]

where \( V_{VSS} = V_A + \varphi_{\text{Sr}} \) is the built-in voltage at source/channel interface, \( \varphi_{\text{Sr}} \) is the Fermi level in the channel and \( V_A \) is a constant parameter for all structures.

The introduction of the SCE in the threshold voltage as roll-off, DIBL and also in the subthreshold slope is done by calculating an effective gate voltage \( V_{\text{Geff}} \), which depends on the minimum potential and is expressed as:

\[
V_{\text{Geff,S,D}} = V_C + \varphi_{\text{Sr}} - \varphi_{\text{Sr}}.
\]

The threshold voltage roll-off is given by evaluating the minimum of potential at \( V_{\text{th}} = 0 \).

After some algebraic manipulation the expression can be written as:

\[
\Delta V_{\text{th}} = \left| V_{\text{th}} - \left( V_{T0} - V_{T0} + \frac{qN_{D0}}{\varepsilon_S} t_n^2 \right) \right| / \cosh \left( \frac{L}{2t_n} \right),
\]

where \( V_{T0} \) is the long channel threshold voltage defined by (7).

### 2.7. Variable mobility

The effective mobility is determined considering the superposition of two parallel currents, one flowing through the center and the other at the surface of the Si layer. The current at the center shows a constant mobility value \( \mu_0 \), but the current at the surface, which is important when the gate voltage is greater than the flat-band voltage, \( V_{FB} \), reduces as the gate voltage increases, due to surface scattering. Surface mobility can be calculated as [35]:

\[
\mu_s = \frac{\mu_0}{1 + \left[ \theta_1 \left( V_C - V_{FB} \right) + \theta_2 V_{\text{Ddef}} \right] + \frac{1}{2} \left[ 1 + \tanh \left( V_S - V_{FB} \right) \right]}.
\]

where \( \theta_1 \) and \( \theta_2 \) are adjusting parameters defining the mobility degradation for \( V_C > V_{FB} \).

The effective electron mobility, considering the saturation velocity as adjusting parameter, is described as [36]:

\[
\mu_{\text{eff}} = \frac{\mu_s}{\left( \frac{e_k V_{\text{sat}}}{t_{ox}} \right)^2}.
\]

### 2.8. Series resistance

The series resistance due to the source and drain extensions with length \( L_{\text{ext}} \) as is indicated in Fig. 1 can degrade the current drive, this effect must not be neglected even for long channel devices [37]. Considering the current factor \( K = 2 \frac{W}{L} C_{\text{ox}} \mu_{\text{eff}}, \) the sum of the source and drain resistances \( R \) and the adjusting
3. Current calculation

The drain current, taking into account all the electron charge inside the silicon layer (3) is calculated by:

\[ I_D = KK \int_{V_T}^{V_D} q_n dV \]
\[ = KK \int_{V_T}^{V_D} \left[ -\frac{q_n(V_C - V_T - N_{\text{eff}})}{\xi} \right] dV. \quad (26) \]

Integral (26) is calculated analytically following the procedure described in [26], where mobile charge was decoupled into two expressions, one for depletion and one for accumulation regime, obtaining integrals that can be solved analytically. In order to reduce the paper length only the final expressions are reproduced. Expressions for functions \( S_n, S_a, S_p \) and \( S_b \) are defined in Appendix B.

The current in below threshold regime is equal to:

\[ I_{\text{dep-b}} = -KK0.03 \phi_n \left[ \frac{1}{2} \left( q_{\text{in}} - q_{\text{tot}} \right) + \frac{1}{\xi} (S_n(\xi_{x_b}) - S_n(\xi_{x_D})) \right]. \quad (27) \]

where \( q_{\text{in}} = q_{\text{tot}}(V_C, V_{\text{SPD}}); \xi_{\text{SPD}} = \xi(V_C, V_{\text{SPD}}); \)

In above threshold regime, the current is obtained as:

\[ I_{\text{dep-at}} = KK \left[ \frac{q_n}{2} \left( V_D - V_S + 0.01 (1.1 \times 10^{-4} - V_D) \right) + \frac{q_n}{2} (q_{\text{in}} - q_{\text{tot}}) \right] \]
\[ + \frac{1}{\xi} \left( S_n(\xi_{x_b}) - S_n(\xi_{x_D}) \right) - \frac{\phi_n}{\xi} (S_b(V_C) - S_b(V_D)). \quad (28) \]

The current in depletion regime is calculated as:

\[ I_{\text{dep}} = \frac{1}{2} I_{\text{dep-b}} \left[ 1 + \tanh \left[ 30(V_C - V_T - \phi_n) \right] \right]. \quad (29) \]

The current in accumulation regime is calculated as:

\[ I_{\text{acc}} = KK \left[ \frac{q_n}{2} \left( V_D - V_S \right) + \frac{q_n}{2} (q_{\text{in}} - q_{\text{tot}}) \right] \]
\[ + \frac{1}{\xi} \left( S_p(V_C - V_{\text{FB}} - V_S) + q_{\text{in}} \right) \]
\[ - S_p \left( \frac{V_C - V_{\text{FB}} - V_D}{\phi_n} \right). \quad (30) \]

The continuous expression for the total drain current considering both regimes is equal to:

\[ I_{\text{tot}} = \frac{1}{2} I_{\text{dep}} \left[ 1 + \tanh \left[ 100(V_C - (V_{\text{FB}} + V_D)) \right] \right] \]
\[ + I_{\text{acc}} \cdot \frac{1}{2} \left[ 1 - \tanh \left[ 100(V_C - (V_{\text{FB}} + V_D)) \right] \right]. \quad (31) \]

An error lower than 0.6% is obtained by approximating the integrals by these functions.

In expressions (26)–(31) \( V_D \) is substituted by \( V_{\text{eff}} \) from (11).

The drain current is calculated by, using the effective gate voltage, effective drain voltage, variable mobility and analyzed SCE for different DGJLT structures. Only 8 model parameters are required.

4. Model validation

4.1. Simulations

The validation of the model was done by simulations in ATLAS, N-type DGJLTs, using Shirahata variable mobility with a maximum value equal to 1000 cm2/Vs and considering the band width variation with doping concentration dependence as the Slothboim model and consequently the affinity change. The following parameters are common for the different structures: channel width of \( W = 1 \mu m \); metal gate workfunction of 5.2 eV; positive interface charge \( N_s = 5 \times 10^{10} \text{cm}^{-2} \); \( t_s = 2 \text{nm and extensions length } L_{\text{ext}} = 30 \text{ nm with N-type doping concentration of } 10^{20} \text{ cm}^{-3} \). Only structures giving positive threshold voltage were selected. The reason for including structures of 30 nm and channel doping concentration lower than \( 10^{19} \text{ cm}^{-3} \) is explained in [29]. The following DGJLT structures were simulated: 1) \( N_s = 5 \times 10^{19} \text{ cm}^{-3} \) and \( t_s = 15 \text{ nm}; 2) \( N_s = 5 \times 10^{18} \text{ cm}^{-3} \) and \( t_s = 10 \text{ nm and } 3) \( N_s = 1 \times 10^{19} \text{ cm}^{-3} \) and \( t_s = 10 \text{ nm. These three type of structures are introduced in Table 1 with column labeled “N”.

The following channel lengths were simulated: 25, 40, 50, 100, 200, 300 and 500 nm. The extracted model parameters are shown in Table 1. The negative values of \( \phi_n \) in Table 1 are due to the slight increase of the current slope above \( V_{\text{FB}} \), observed in the simulated characteristics.

The transfer characteristics were obtained varying the gate voltage from –0.2 to 1.5 V. The lineal transfer characteristic was simulated for \( V_{\text{DD}} = 50 \text{ mV} \) and the transfer curve in saturation for \( V_{\text{DD}} = 1.5 \text{ V}. \) The output characteristic was obtained for \( V_D \) from -0.2 to 1.5 V and \( V_C = 1 \text{ V} \).

4.2. Analysis of results

To validate the model with the inclusion of short channel effects, simulated and calculated currents have been compared. This comparison was done extracting the device and model parameters shown in Table 1. \( V_T \) was extracted by the second derivative method for lineal region and \( \Delta V_T \) from the \( I-V \) curve shift. The DIBL was extracted using:

\[ \text{DIBL} = \frac{V_{T1}(V_{D1}) - V_{T1}(V_{D2})}{V_{D2} - V_{D1}} \]

for \( V_{D2} = 1.5 \text{ V}; V_{G1} = 0.05 \text{ V}. \)

The subthreshold slope \( S \) was calculated from:

\[ S = \frac{V_{G2} - V_{G1}}{\log(I_{D1}) - \log(I_{D2})}, \]

with \( V_{G2} = 0 \) and \( V_{G2} = 0.1 \text{ V} \) for the structures DGJLT 1 and 3, for DGJLT 2 the selected gate voltages are \( V_{G1} = 0.2 \text{ V} \) and \( V_{G2} = 0.3 \text{ V} \) due to its greater threshold voltage.

<table>
<thead>
<tr>
<th>( N )</th>
<th>( L ) (nm)</th>
<th>( \mu_0 ) (cm2/Vs)</th>
<th>( R ) (( \Omega ))</th>
<th>( n )</th>
<th>( \theta_1 ) (V(^{-1}))</th>
<th>( \theta_2 ) (V(^{-1}))</th>
<th>( n_{\text{sat}} \times 10^7 ) (cm/s)</th>
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The extracted $S$ and DIBL versus channel length, for simulated and modeled data are shown in Fig. 2.

Figs. 3 and 4 show the comparison between simulated and modeled normalized transfer characteristics for a structure with silicon layer of $t_s = 15$ nm and $N_D = 5 \times 10^{18}$ cm$^{-3}$, at $V_D = 50$ mV and $V_D = 1.5$ V, in natural and semilog scales. The normalized transconductance for the lineal and saturation regimes are shown in Fig. 5. The transconductance efficiency $g_m/I_D$ is shown in Fig. 6, where the maximum values are equal to the theoretical value of $1/\mu t S^2$ for $L = 100$ nm. The normalized output characteristics and the output conductance are shown in Fig. 7.

The model was also validated for other two structures with $t_s = 10$ nm and doping concentration of $5 \times 10^{18}$ and $10^{19}$ cm$^{-3}$, obtaining similar results to the previously modeled structure.

In order to avoid a large quantity of figures only the comparison between the three analyzed structures with a channel length of 40 nm has been presented and one more validation for the most heavily doped structure at channel length of 25 nm.

Fig. 8 compares transfer characteristics at $V_D = 50$ mV and Fig. 9 at $V_D = 1.5$ V. Fig. 10 shows transconductance at $V_D = 50$ mV and

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Fig. 2. Subthreshold slope and drain induced barrier lowering versus channel length.

Fig. 3. Simulated and modeled transfer characteristics in subthreshold and lineal scale at $V_D = 50$ mV.

Fig. 4. Simulated and modeled transfer characteristics in subthreshold and lineal scale at $V_D = 1.5$ V.

Fig. 5. Simulated and modeled transconductance at $V_D = 50$ mV (left axis) and $V_D = 1.5$ V (right axis).

Fig. 6. Simulated and modeled transconductance efficiency at $V_D = 1$ V.
Fig. 7. Simulated and modeled output characteristics (right axis) and output conductance at $V_G = 1\, \text{V}$ (left axis).

Fig. 8. Comparison of simulated and modeled transfer characteristics in subthreshold and linear scale at $V_D = 50\, \text{mV}$ for four different structures.

Fig. 9. Comparison of simulated and modeled transfer characteristics in subthreshold and linear scale at $V_D = 1.5\, \text{V}$ for four different structures.

Fig. 10. Comparison of simulated and modeled transconductance at $V_D = 50\, \text{mV}$ (left axis) and $V_D = 1.5\, \text{V}$ (right axis) for four different structures.

Fig. 11. Comparison of simulated and modeled output characteristics (right axis) and output conductance (left axis) at $V_D = 1\, \text{V}$ for four different structures.

Fig. 12. Comparison of simulated and modeled transfer characteristics in subthreshold and linear scale at $V_D = 1\, \text{V}$ for four different structures.

From these figures we can conclude that there is an excellent coincidence between simulated and modeled characteristics in all operation regions, as well as continuity of the current and its derivatives for different silicon layer thicknesses, doping concentrations and channel lengths. Model describes very well the behavior of short-channel DGJLTs, as can be seen from the transconductance curves in the linear region in Figs. 5 and 10, where the transition between operating regimes takes place. Model guarantees the symmetry around the condition of $V_D = 0\, \text{V}$ for the current at its derivatives, as was shown in [26]. The consideration of the minimum of potential along the channel in the effective gate voltage allows the correct description of the $V_T$ roll-off, the subthreshold slope variation and DIBL with the channel length and the drain voltage.

5. Conclusions

A compact analytical model for double-gate Junctionless short-channel MOSFET is presented considering different silicon layer thicknesses, doping concentrations and channel lengths. Drain saturation voltage is obtained semi-empirically and the
potential is solved by third order Newton–Raphson’s method with a proposed initial guess value. This value gives the desire result in the first iteration and makes the model robust and fast. The short-channel effects included in the model are variable mobility, threshold voltage roll-off, subthreshold slope variation, DIBL, channel shortening and saturation velocity. Modeled transfer and transconductance characteristics in linear and saturation regions; output characteristics; output conductance and transconductance characteristics in linear and saturation regions; threshold voltage roll-off, subthreshold slope variation, DIBL, short-channel effects included in the model are variable mobility, potential is solved by third order Newton–Raphson’s method with a possible approach to the solution. The following algorithm was developed as a second step, a more accurate solution is calculated iteratively as follows:

$$x_{n+1} = x_n + g(x_n).$$

As a second step, a more accurate solution is calculated iteratively as follows:

$$x_{n+1} = x_n + g(x_n).$$

The function $g(x)$ is a third order adjustment to the root’s position. An initial point $x_0$ is needed to estimate the offset required to approach to the solution. To ensure the convergence and reduce the amount of iterations this value is supposed to be as close as possible to the solution. The following algorithm was developed to establish a very good starting point:

$$q_{a} = -x_0 \left( e^{x_0} - 1 \right): q_x + q_{ap}$$

$$v_1 = (V_G - V_{th} - V_D)/\varphi_t$$

$$v_2 = v_1 + 0.8 \beta$$

$$x_{a} = \frac{q_{a} - V_D}{\varphi_t}$$

$$x_{d} = v_1 - \frac{\beta}{2} \left( 1 - \sqrt{1 - \frac{4}{\beta} (v_1 + 1)} \right) + 0.7$$

$$x_{fr1} = x_{a} \frac{1}{2} \left[ 1 - \tanh \left[ 50 (V_G - V_T) \right] \right] + x_{fr2} \frac{1}{2} \left[ 1 + \tanh \left[ 50 (V_G - V_T) \right] \right]$$

$$x_{fr2} = v_2 - 2 LW \frac{1.09}{2} \beta \exp (v_2/2) + 0.7$$

$$x_0 = x_{fr1} \frac{1}{2} \left[ 1 - \tanh (50 \cdot v_1 \varphi_t) \right] + x_{fr2} \frac{1}{2} \left[ 1 + \tanh (50 \cdot v_1 \varphi_t) \right],$$

(A6)

where $\varphi_{ap}$ and $\varphi_a$ are the subthreshold long channel potentials at the center and surface of the silicon layer, respectively and $t_n$ is the natural length obtained by using the approximation of Poisson equation in subthreshold regime:

$$t_n = \frac{t_s}{\sqrt{8 \left( 1 + \frac{1}{y} \right)}}$$

(A7)

In this regime, the surface potential is calculated also without iterations. The constants used in (A7) were obtained for improving the convergence.

By using this first approximation the process defined by (A6) converges to a fixed point in one or two iterations with a negligible error.

**Appendix B**

In this appendix, the set of definitions of functions $SaN$, $SaP$ and $Sb$ are presented.

$$SaN(z) = \sum_{n=0}^{5} z^{2n}$$

(B1)

$$SaP(z) = \sum_{n=0}^{5} z^{2n}$$

(B2)

$$Sb(z) = \left\{ \begin{array}{ll}
\sigma_0 \ln (z - x_0) - \sigma_1 |z + x_0 \ln (z - x_0)| + \frac{4}{n+1} \sigma_2 \frac{x^{n+1}}{n+1} \end{array} \right\}$$

(B3)

with $x_0 = \frac{z}{x_n}$ and $fhyper$ is the gauss hypergeometric function implemented successfully with an adaptive algorithm. Coefficients $\zeta$, $\chi$ and $\sigma$ are indicated in [26].

**References**


