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Effects of interface trap density on the electrical performance of amorphous InSnZnO thin-film transistor

Liang Yongye(梁永焯)^{1,2}, Kyungsoo Jang², S. Velumani³, Cam Phu Thi Nguyen², and Junsin Yi^{2,†}

¹National Key Laboratory for Electronic Measurement Technology, North University of China, Taiyuan 030051, China

²College of Information and Communication Engineering, Sungkyunkwan University, 300 Chunchun-dong, Jangan-gu, Suwon, Gyeonggi-do 440-746, Republic of Korea

³Department of Electrical Engineering (SEES), CINVESTAV-IPN, Avenida IPN 6508, San Pedro Zacatenco, Mexico D.F.

Abstract: We reported the influence of interface trap density (N_t) on the electrical properties of amorphous InSnZnO based thin-film transistors, which were fabricated at different direct-current (DC) magnetron sputtering powers. The device with the smallest N_t of $5.68 \times 10^{11} \text{ cm}^{-2}$ and low resistivity of $1.21 \times 10^{-3} \Omega\text{-cm}$ exhibited a turn-on voltage (V_{ON}) of -3.60 V , a sub-threshold swing (S.S) of 0.16 V/dec and an on-off ratio (I_{ON}/I_{OFF}) of $\sim 8 \times 10^8$. With increasing N_t , the V_{ON} , S.S and I_{ON}/I_{OFF} were suppressed to -9.40 V , 0.24 V/dec and 2.59×10^8 , respectively. The V_{TH} shift under negative gate bias stress has also been estimated to investigate the electrical stability of the devices. The result showed that the reduction in N_t contributes to an improvement in the electrical properties and stability.

Key words: a-ITZO TFTs; low resistivity; interface trap density; electrical properties; electrical stability

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1. Introduction

Thin film transistors (TFTs) using transparent amorphous semiconductors are considered as an attractive alternative to conventional silicon based TFTs. Next generation flat plane displays using amorphous oxide semiconductors are state of the art technology, which is attracting huge attention in semiconductor industries. TFT's on flexible substrates is a key component to realize flexible electronics, which will be indispensable in near future ubiquitous network technology, as they can be used to develop advanced optoelectronic devices^[1]. Good transparent conducting oxides (TCOs) due to their wide optical band gap (3.5 eV), good electrical conductivity ($10^3 \Omega/\text{cm}$), and high optical transparency (80%)^[2] have been widely used in various applications. TFT's with ZnO thin films as an active channel layer were fabricated by atomic layer deposition (ALD)^[3] and the radio frequency (RF) magnetron sputtering technique^[4-6]. Also, gallium doped zinc oxide (GZO)^[7,8], indium zinc oxide (IZO)^[8,9], indium-tin-oxide (ITO) films^[8] and amorphous InGaZnO (a-IGZO)^[10,11] have also been reported. Zinc based TCOs can solve the problems of cost and demand compared to indium based TCOs, which showed better electro-optical properties but with a higher cost^[8]. There are several reports about transparent TFTs using various TCOs with low resistivity in the channel region for high performance. Jang *et al.*^[12] reported that the TFTs using AZO as the active layer with low resistivity shows an on/off current ratio of 10^4 and a field-effect mobility of $0.17 \text{ cm}^2/(\text{V}\cdot\text{s})$. Paine *et al.*^[13] also showed a-IZO-based TFT devices with a low resistivity of $5.96 \times 10^{-4} \Omega\text{-cm}$, which perform on/off ratios above 10^6 and a sub-threshold slope of 1.2 V/decade . Huang *et al.*^[14] investigated that when the resistivity of TZO thin films is 3×10^{-3}

$\Omega\text{-cm}$ (deposition power 125 W), NiO/TZO heterojunction devices with the turn-on voltage of 1.83 V . However, at low resistivity, there is still a large off-current and a sub-threshold slope.

InSnZnO (ITZO) has attracted considerable attention as a promising material to be developed not only for ultra high-definition displays such as 4k/8k panels and 3D displays^[15], but also for driver circuits, memory devices and charge coupled devices^[16]. Amorphous ITZO (a-ITZO) films which have a smooth surface, low internal stress and high etchability for applications to next-generation displays have been investigated^[17]. The a-ITZO films deposited on a polyimide substrate at high temperatures^[18] and polyethylene terephthalate (PET) by magnetron co-sputtering using two cathodes (DC, RF) at room temperature^[19] have been reported in some studies. The a-ITZO is also one of the promising candidates for an active channel layer of TFTs^[20]. For improving characteristics of a-ITZO TFTs, more investigations and analyses of the a-ITZO thin films are needed. Therefore, this paper presents the characteristics of TFTs with an a-ITZO active channel layer, which shows low resistivity but improved electrical performance. The ITZO films were deposited by different DC magnetron sputtering, which is the main deposition method because of its high output and good stability^[21] at room temperature. The interface trap density (N_t) is one of the main determinants for transistor performance. It is found that there is a noticeable interrelationship between the electrical performances and N_t ^[22]. Therefore, the influence of the interface trap density (N_t) existing at the channel/dielectric layer interface on the electrical characteristics and stabilities of a-ITZO TFTs is clearly established. This helps in diagnosing fabrication processes and optimizing these

† Corresponding author. Email: yi@yurim.skku.ac.kr

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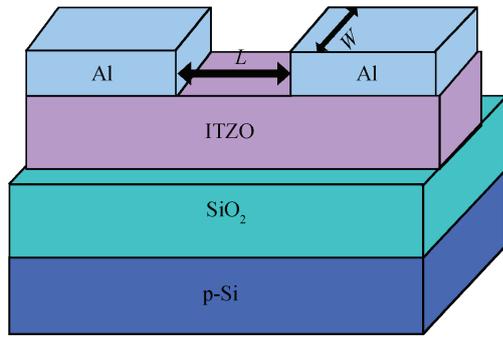


Figure 1. Schematic cross-sectional diagram of the a-ITZO TFT bottom-gate structure.

parameters effectively in order to obtain the ascending performances of the TFT devices.

2. Experimental

The a-ITZO-based TFT device with the schematic cross section is presented in Figure 1. In this study, the a-ITZO thin films were grown onto a p-type-crystalline silicon (p-Si) substrate coated with a 100 nm thick SiO₂ gate dielectric layer, which were fabricated by the oxidation method. Thermal oxidation of silicon is achieved by heating the wafer to a high temperature, typically 900 to 1200 °C. The p-Si and SiO₂ acted as the gate electrode and gate insulator, respectively. All substrates were cleaned by acetone, iso-propylalcohol and de-ionized water in an ultrasonic bath for 10 min. A 100 nm-thick SiO₂ insulator for the TFTs was produced on the p-Si gate electrode. Then, a 30 nm thick ITZO layer was deposited on the SiO₂ insulator at different input powers of 80 W, 120 W and 160 W with a 30 : 35 : 35 mol indium oxide (In₂O₃) : tin oxide (SnO₂) : zinc oxide (ZnO) composition. All the depositions were carried out under an Ar atmosphere and the working pressure was 5 mTorr at room temperature. The final devices were annealed at 350 °C for 1 h under air ambience. For the source and drain electrodes, 150 nm thick Al layers were deposited by thermal evaporation. The S/D electrodes and the active layer were patterned via the standard photolithography method using a two masks patterning process. The channel width (*W*)/length (*L*) was 200/200 μm for TFT measurements. In this paper, we assign the names of the samples A, B and C for the TFTs with a-ITZO films sputtered deposited at powers 80 W, 120 W and 160 W, respectively. A semiconductor test and analyzer model number EL420C was used to measure the electrical characteristics of TFTs. The structural properties of the ITZO thin film were characterized using X-ray diffraction (XRD, Bruker D8 Discovery). The thickness of a-ITZO films was measured by an ellipsometer (J.A Woollam, VASE-VB250).

3. Results and discussion

It can be confirmed that the XRD patterns of all the samples were in the form of halo patterns^[18, 19] (data not shown), indicating that all the ITZO thin films have an amorphous structure. Figure 2 shows the plot of log(*I*_{DS})-*V*_{GS} transfer characteristic of all devices with the gate voltage (*V*_{GS}) swept

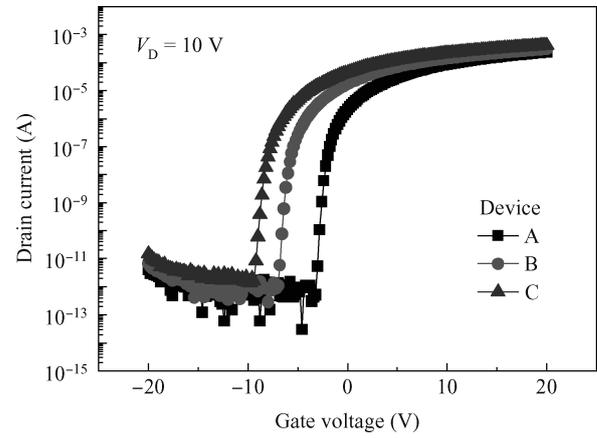


Figure 2. Transfer characteristics log(*I*_{DS})-*V*_{GS} at *V*_{DS} = 10 V of a-ITZO TFTs for devices A, B and C.

from -20 to 20 V and the drain voltage (*V*_{DS}) fixed at 10 V. The parameters, sub-threshold swing (SS), turn-on voltage (*V*_{ON}), threshold voltage (*V*_{TH}), on-off current ratio (*I*_{ON}/*I*_{OFF}), and interface trap density (*N*_t) of the devices are extracted from the plotted curves and summarized in Table 1. The extraction methods are reported elsewhere by our group^[23].

From Table 1, it is observed that sample A, sputter deposited at 80 W, has the smallest on-voltage (*V*_{ON}) of -3.60 V, the highest on-off current ratio (*I*_{ON}/*I*_{OFF}) of 7.77 × 10⁸ and the lowest SS of 0.16 V/dec. The *V*_{ON} value is shifted to -7.19 and -9.40 V for samples B and C respectively, at which the drain current begins to increase sharply above the leakage current^[24]. The improvement in the electrical properties of device A reveals the termination of defects at the a-ITZO/dielectric interface and in the a-ITZO bulk. The value of the interface state density (*N*_t) is presented as^[22, 25]

$$N_t = \frac{SS \log_{10} e C_i}{kT/q}, \quad (1)$$

where *q* is the elementary charge, *k* is Boltzmann's constant, *T* is the absolute temperature, *t* is the thickness of the channel layer, and *C*_i is the gate capacitance per unit area. These results indicate that a lower *N*_t can improve *V*_{ON}, owing to the reduction in the trap amount in a-ITZO film and at the gate dielectric/a-ITZO film interface.

The resistivity of a-ITZO films is evaluated from the current-voltage (*I*-*V*) measurement plot shown in Figure 3. The resistivity of the a-ITZO single layer is estimated using the following equation^[26]:

$$\rho = \frac{V}{I} \frac{W}{L} t, \quad (2)$$

where *V* denotes the input voltage, *I* is the output current, and *W* and *L* denote the width and length of the electrode, respectively, where *t* is the thickness of the ITZO layer. From Figure 4, we can see that the electrical resistivity decreased from 1.21 × 10⁻³ to 2.49 × 10⁻⁴ Ω as the DC power is increased from 80 to 160 W. This result can be interpreted based on the fact that, the oxygen vacancies in the a-ITZO bulk are the predominant factor for the conduction mechanism^[27]. The

Table 1. Comparison of the extracted electrical properties including SS, V_{ON} , V_{TH} , I_{ON}/I_{OFF} , N_t and ρ .

Device	SS (V/dec)	V_{ON} (V)	V_{TH} (V)	I_{ON}/I_{OFF}	N_t (cm ⁻²)	ρ (Ω -cm)
A	0.16	-3.60	-1.87	7.77×10^8	5.68×10^{11}	1.21×10^{-3}
B	0.19	-7.20	-5.35	3.51×10^8	1.10×10^{12}	2.14×10^{-4}
C	0.24	-9.40	-7.81	2.59×10^8	2.11×10^{12}	2.49×10^{-4}

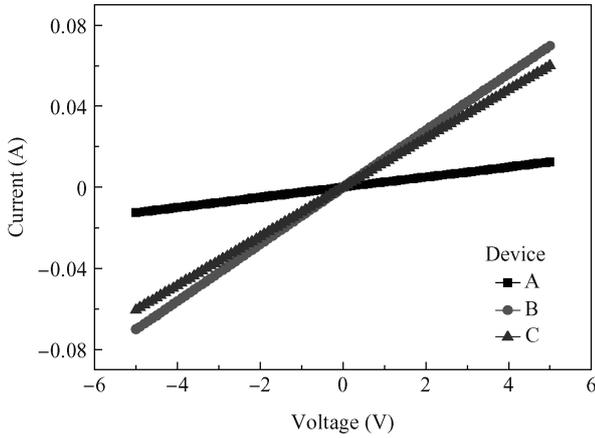


Figure 3. The characteristic of input voltage–output current for all devices.

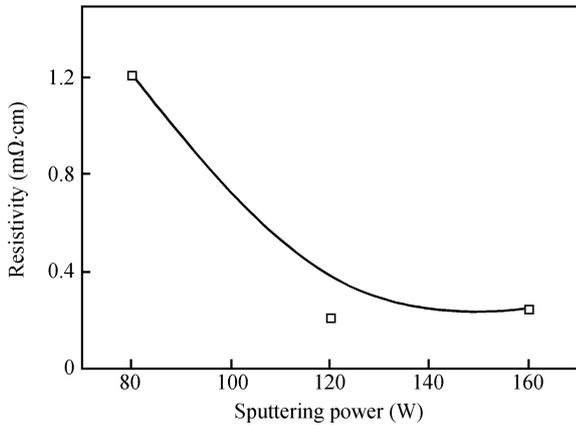


Figure 4. The changes in resistivity as a function of sputtering power.

increased sputtering power tends to increase the film deposition rate^[21], which makes the oxidation reaction insufficient and more oxygen vacancies are created. Oxygen vacancies are the major source of free carriers in amorphous oxide semiconductor TFTs, which can affect the oxygen concentration within the active layer^[28]. Therefore, the enhancement in oxygen vacancies leads to the resistivity of a-ITZO being reduced.

The SS is another important advantageous parameter for the evaluation of TFT, which can predict the total trap density of the TFT's performance. Figure 5 depicts the variation of SS and I_{ON}/I_{OFF} of a-ITZO TFT devices with different sputtering powers, ranging from 80 to 160 W. The best SS value of 0.156 V/dec was obtained for sample A with the lowest N_t . This reveals that improved SS is related to the reduction in the interface trap density (N_t) at the interface between the active layer and the insulator^[26]. It can also be clearly seen that, as N_t increases, SS also increases while the I_{ON}/I_{OFF} ratio decreases. The carriers could transfer more smoothly without be-

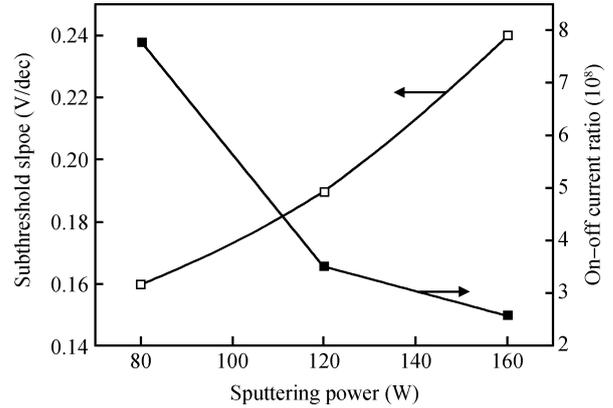


Figure 5. Electrical properties of a-ITZO-based TFTs as a function of sputtering power.

ing trapped in the defect centers, which led to the large turn-on current and the smaller threshold voltage^[29]. This version can be verified by the on-off current ratio improved from 2.60×10^8 to 7.77×10^8 with the trap density decreased in this paper.

In order to guarantee the effect of the device stability, we have applied negative gate bias stress (NGBS) $V_G = -15$ V to the a-ITZO TFTs at room temperature for 10^4 s duration while the source and drain are grounded. The bias is interrupted at fixed times to record the transfer curve (shown in Figure 6) of the transistors, by sweeping V_{GS} from -20 to 20 V. The V_{TH} at 10^4 s for devices A, B and C are shifted to the negative direction by -2.45, -3.38 and -3.69 V, respectively (shown in Figure 7(a)). All samples showed that the SS has no obvious variation with increasing stress, as shown in Figure 7(b). The parallel shift in V_{TH} without significant change in the SS value during stress time indicates the simple charge trapping process in the gate insulator and/or at the channel/insulator interface^[26]. However, in our experiment, we used the SiO₂ commercial insulator which has a high quality with low interface traps. Therefore, the shift in V_{TH} has been explained as being due to the charge trapping at the active channel/insulator interface. Besides, holes could be easily moved from the channel to the gate dielectric by stresses such as the applied bias. However, the low interface trap charges make the holes difficult to move when stresses are applied^[20]. All the above can be confirmed by the result that sample A with the slightest N_t showed the least ΔV_{TH} . When the devices were sputtered at a lower power, the number of interface traps decreased, therefore, the ΔV_{TH} reduced. Sample A shows both a low SS and ΔV_{TH} , insinuating a reduction in defects at the a-ITZO active layer/insulator interface; this sample demonstrated the best stability with negative bias stress compared to the other devices.

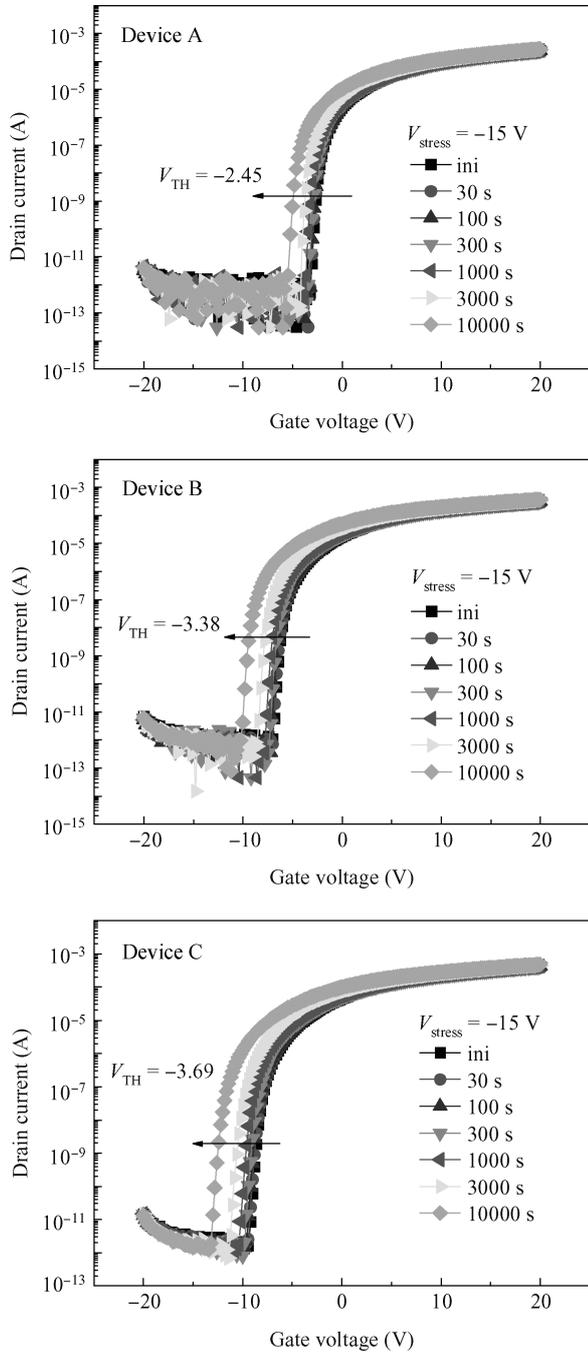


Figure 6. Transfer curves as a function of NGBS for devices A, B and C.

4. Conclusion

In this study, the effect of the interface trap density (N_t) on the electrical properties and stability of staggered bottom-gate a-ITZO TFTs has been investigated. The electrical properties of the a-ITZO TFT devices such as turn-on voltage (V_{ON}), subthreshold swing (SS) and on-off ratio (I_{ON}/I_{OFF}) are influenced with a different N_t by controlling the sputtering power. The interface trap density increases as the sputtering power is increased. In our investigation, the best TFT parameters are observed with the lowest interface trap density of $5.68 \times 10^{11} \text{ cm}^{-2}$, like $V_{ON} = -3.60 \text{ V}$, $SS = 0.16 \text{ V/dec}$ and with an on-off current ratio of over 10^8 even the resistivity is low. The

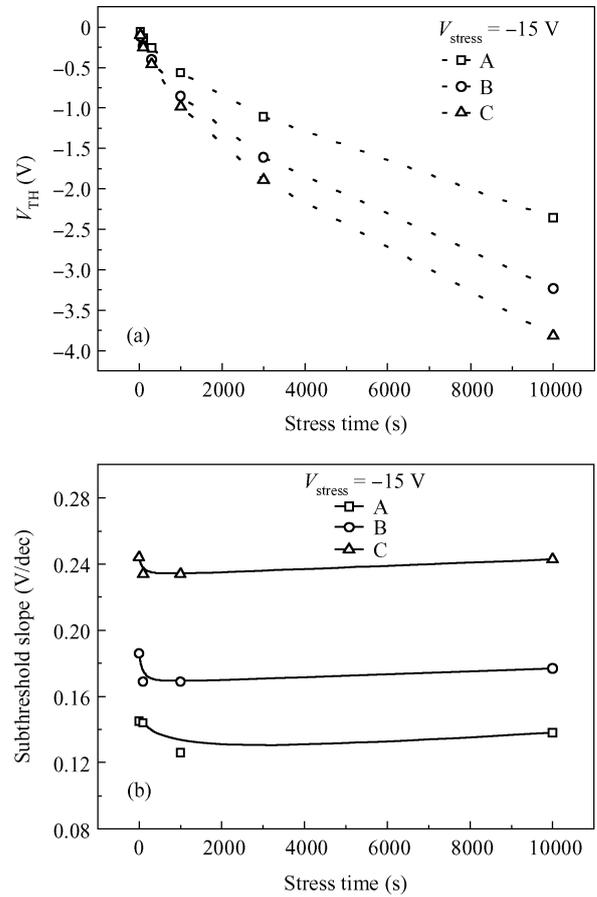


Figure 7. (a) The V_{TH} shift with gate bias stress time for all devices. (b) The SS shift with gate bias stress time for all devices.

slight threshold voltage shift is observed with device A under negative gate bias stress, while it exhibits the lowest N_t . From the results of this study, it is shown that the electrical characteristics and stability of the resulting TFTs can be improved by reducing the N_t through changing the deposition conditions. The method such as changing the O_2/Ar gas flow ratio or other experimental conditions to obtain a lower N_t are being studied and confirmation is underway.

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