A compact model and direct parameters extraction techniques for amorphous gallium-indium-zinc-oxide thin film transistors

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Abstract
An advanced compact and analytical drain current model for the amorphous gallium indium zinc oxide (GIZO) thin film transistors (TFTs) is proposed. Its output saturation behavior is improved by introducing a new asymptotic function. All model parameters were extracted using an adapted version of the Universal Method and Extraction Procedure (UMEM) applied for the first time for GIZO devices in a simple and direct form. We demonstrate the correct behavior of the model for negative VDS, a necessity for a complete compact model. In this way we prove the symmetry of source and drain electrodes and extend the range of applications to both signs of VDS.

The model, in Verilog-A code, is implemented in Electronic Design Automation (EDA) tools, such as Smart Spice, and compared with measurements of TFTs. It describes accurately the experimental characteristics in the whole range of GIZO TFTs operation, making the model suitable for the design of circuits using these types of devices.

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1. Introduction
Transparent amorphous oxide semiconductor (AOS) materials have become of great interest for electronic device applications, i.e. thin film transistors (TFTs), electronic papers, sensors, etc., due to their promising characteristics such as large electron mobility, low temperature process, large area fabrication, low cost, and compatibility with flexible electronics [1,2]. Specifically, AOS TFTs have several features that make them attractive for applications in flexible flat-panel displays and large-area integrated circuits [3]. Among these, Ga-In-Zn-O (GIZO) TFTs have resulted very promising for switching devices in high-resolution active matrix liquid crystal displays (AMLCDs) with high frame rate and for current-driving devices in large-size active-matrix organic light-emitting diode (AMOLED) displays due to their high field-effect mobility, low off current, and excellent short-range uniformity [3–6]. Nevertheless, it is well known that, to obtain efficient circuits based on any device, preliminary modeling for circuit simulation is necessary.

In the last years, both numerical and analytical compact models for GIZO TFTs have been proposed. Even though several numerical models have been presented [7–11] they were not time efficient and so, not suitable for circuit simulation. Empirical models based on artificial neural networks (ANNs) were also demonstrated for this transistor technology, enabling accurate and continuous models but having parameters lacking explicit physical meaning [12].

On the other hand, compact models [13–15] are focused on the accurate physical-based description of the transistor’s characteristics. Different methods are implemented to develop an analytical current–voltage model. In [14] is presented a GIZO current model based on MOSFET equations. Also, the surface potential based models, like [16] are not efficient for large display circuits design. However, since AOS TFTs are based on a TFT structure similar to a-Si TFTs and the active layer is also amorphous, it seems that their behavior should be closer to that of a-Si:H TFTs [17–19]. On the other hand no direct parameter extraction methods have been presented for amorphous GIZO TFTs.
Here we present an advanced compact model for AOS TFTs valid for GIZO devices and based on the physical behavior of the device, with an adequate consideration of its Density of States (DOS).

Our model is based on the unified model and extraction method (UMEM), which has been validated with devices made of different materials [17,20,21] and is applied for the first time to GIZO devices. The parameters are easily extracted from the experimental measurements with no need of using optimization methods. The model will include an improved asymptotic function for the saturation behavior [22] and an extended range of applications due to its proven symmetry of source and drain electrodes.

We implemented the GIZO model’s Verilog-A code in Smart Spice and it is shown that a good agreement is obtained with experimental data. The presented model also, displays a smooth transition between the different regimes of operation of the TFT.

2. Experimental device

The GIZO TFTs on Si/SiO2 substrates were fabricated and characterized at the Universidade Nova de Lisboa (UNL). Fig. 1(a) shows the schematic structure of the device with channel width \( W = 160 \mu \text{m} \) and channel length \( L = 20 \mu \text{m} \), while the real GIZO TFT is shown in Fig. 1(b) [23].

The TFTs used in this work are fabricated with a staggered bottom gate top-contact structure, on a 5 layer process (gate electrode, dielectric, oxide semiconductor, source/drain electrodes, passivation).

All the layers except passivation (which is spin-coated SU-8) are produced by sputtering without intentional substrate heating, being patterned using conventional photolithography. Devices are annealed at 150°C on a hot plate, for 1 h. Other processing details for the active layer electrodes of the TFTs were previously reported elsewhere [24,25].

Static electrical characterization measurements were was performed with a probe station (Janis ST500) and a semiconductor parameter analyzer (Keithley 4200 SCS), in the dark, at room temperature, and in air atmosphere [26].

3. TFT modeling

The distribution of acceptor-type localized states in the mobility band of an amorphous n-type inorganic TFT is represented as the sum of the tail and deep states, which are exponentially dependent on the energy:

\[ g_a = g_{aso} \exp \left( \frac{E_a - E_g}{kT_1} \right) + g_{ado} \exp \left( \frac{E_a - E_g}{kT_2} \right) \]  

where \( g_{aso} \) and \( g_{ado} \) are the tail and deep acceptor densities extrapolated at \( E = E_g \) and \( E_s \) is the conduction band energy; \( T_1 \) and \( T_2 \) are the characteristic temperatures of the tail and deep states respectively and \( k \) is the Boltzmann constant.

3.1. Above threshold regime

Typically, in amorphous TFTs the field effect mobility above threshold \( (V_{DS} > V_T) \) is well represented by the power law equation [27,28]:

\[ \mu_{EFF} = \frac{\mu_0}{V_{sat}^{\gamma_a}} (V_{DS} - V_T)^{\gamma_a} \]

where \( V_T \) is the threshold voltage, \( V_{sat} \) and \( \gamma_a \) are parameters defining the variation of mobility with gate bias in the above threshold condition, and are extracted by UMEM according to [17]. \( \mu_0 \) is used for dimensional purposes and is taken as 1 cm²/Vs.

3.1.1. Output asymptotic behavior

The output conductance is usually modeled by multiplying the total current by \((1 + \lambda V_{DS}) \) [28], where \( \lambda \) is the saturation coefficient. Its physical origin is related to the channel length modulation and defines the non-ideal output curve at high \( V_{DS} \).

According to this standard procedure, the asymptotic current will be calculated as \( I_{AS} = I_{sat} (1 + \lambda V_{DS}) \), where \( I_{sat} \) is the current in saturation. The output asymptote \( I_{AS} \) defines a higher current than the actual one, which gradually tends to the asymptotic current as \( V_{DS} \) becomes sufficiently high.

The disadvantage of this approach is that the currents \( I_{sat} \) and the real \( I_{DS} \) are too far apart and in general this gives rise to an inaccurate prediction of the low-voltage output conductance [29].

In order to overcome this problem, a different multiplication factor is proposed [22] giving a new asymptotic current \( I_{AS} = I_{sat} (1 + \lambda V_{DS} - V_{sat}) \), where \( V_{sat} \) is the saturation voltage and \( \lambda_s \) is the saturation parameter that defines the saturation voltage. In this case \( I_{AS} \) is closer to \( I_{DS} \), so the fitting accuracy is improved not only for the \( I_{DS} \) but also for the output conductance, which is an important parameter for analog circuit simulations.

This method [22], prevents unexpected overestimation of low \( V_{DS} \) conductance by reducing the contribution of the asymptotic term in the linear regime.

We also include the function \( V_{DS} \) which only enables a smooth transition between linear and saturation regimes and it will be approximately equal to \( V_{sat} \) when \( V_{DS} < V_{sat} \) and approximately equal to \( V_{DS} \) when \( V_{DS} \) >> \( V_{sat} \).

\[ V_{DS} = V_{DS} \left( 1 + \frac{V_{DS} - V_{sat}}{V_{sat}} \right)^{\frac{1}{\gamma}} \]  

Fig. 1. (a) a-GIZO TFT structure, and (b) Fabricated device with \( W = 160 \mu \text{m} \), \( L = 20 \mu \text{m} \) [23].
where \( m \) adjusts the sharpness of the knee region of transition between linear and saturation regions.

We consider the absolute values of \( V_{DS} \) and \( V_{S} \) in order to extend the range of applications to both signs of \( V_{DS} \).

Finally, the drain current in GIZO TFT above threshold regime is expressed based on [17,21] and including the new saturation asymptotic term.

\[
I_{DS}(V_{GS}, V_{DS}) = K \frac{V_{CS} - V_{FB}}{1 + KR(V_{CS} - V_{FB})^{1+\gamma} - V_{DS}} \left[ \frac{V_{DS}}{1 + \lambda |V_{DS} - V_{DSE}|} \right]^{\frac{m}{1+\lambda}}
\]

(4)

where \( K = \frac{W}{C_{G}} \), \( W \) and \( L \) are the device channel width and length respectively; \( C_{G} \) is the gate capacitance per unit area and \( R \) is the sum of source and drain contact resistances. These parameters are extracted by UMEM [20,30].

### 3.2. Subthreshold regime

In subthreshold, the drain current can be described as [31]:

\[
I_{DS}(V_{GS}, V_{DS}) = K \frac{V_{CS} - V_{FB}}{1 + KR(V_{CS} - V_{FB})^{1+\gamma} - V_{DS}} \left[ \frac{V_{DS}}{1 + \lambda |V_{DS} - V_{DSE}|} \right]^{\frac{m}{1+\lambda}}
\]

(5)

where \( V_{FB} \) is the flat band voltage and \( V_{DSE} \) is a transition term, and it will be equal to:

\[
V_{DSE} = V_{DS} \left[ 1 + \left( \frac{V_{DS}}{2(V_{CS} - V_{FB})} \right)^{m} \right]^\frac{1}{\lambda}
\]

(6)

where \( \lambda = 0.8 \). \( V_{FB} \) and \( \gamma \) are parameters defining the variation of mobility with gate bias in the subthreshold regime and are extracted analytically according to [17]; \( \gamma \) depends on the temperature \( T \) and on the characteristic temperature of the deep states distribution (\( T_{2} \)) (See Eq. (1)).

\[
\gamma = 2 \left( \frac{T_{2}}{T} - 1 \right)
\]

(7)

Well below \( V_{T} \), in deep subthreshold regime where \( I_{DS} \) can no longer model the drain current, diffusion becomes the predominant charge transport mechanism and the current shows an exponential dependence with the gate voltage which can be expressed as [32]:

\[
I_{L} = I_{0} \frac{V_{CS} - V_{FB}}{1 + \gamma_{0} |V_{CS} - V_{FB}|^{3}}
\]

(8)

\( V_{L} \) is selected so that the value \( V_{FB} + V_{L} \) is slightly over \( V_{FB} \) to provide a satisfactory sewing of \( I_{L} \) and \( I_{DS} \). \( V_{L} \) is the subthreshold slope for the linear and transfer curve. Its value is determined by calculating the slope of the experimental curve in the region where the \( I_{DS} \) vs. \( V_{CS} \) in semi logarithmic plot is linear for \( V_{CS} < (V_{FB} + V_{L}) \).

Firstly, both parts of the subthreshold region will be sewed together (Eqs. (5) and (8)).

\[
I_{L} = I_{0} \left[ \frac{1 - \tanh [(V_{CS} - (V_{FB} + V_{L}))Q_{L}]}{2} \right]^{\frac{1}{\lambda}}
\]

(9)

where \( Q_{L} \) is the parameter defining the weight of the tanh function applied to each part of the total current.

Finally, the expression to model the total drain current consists in binding the above threshold, subthreshold, and deep subthreshold regions, i.e. \( I_{0} \) and \( I_{L} \) and \( I_{DS} \), and in adding the off-current \( I_{0} \).

In this case we considered a constant current \( I_{0} \) of \( 10^{-6} \) A.

Thus, the total drain-to-source current is described by (10), with a positive sign for n-channel TFTs, whereas a negative one for p-channel devices.

\[
I_{DS} = \pm \left[ I_{0} + I_{ab} \left( \frac{1 - \tanh [(V_{CS} - (V_{FB} + V_{L}))Q_{ab}]}{2} \right) + I_{ab} \left( \frac{1 + \tanh [(V_{CS} - (V_{FB} + V_{L}))Q_{ab}]}{2} \right) \right]
\]

(10)

\( V_{0} \) and \( Q_{0} \) are adjusting parameters. \( V_{0} \) is selected so that the value \( V_{CS} + V_{0} \) is slightly over \( V_{T} \) to provide a satisfactory sewing point of both regions; and \( Q_{0} \) modifies the weight of the tanh function applied to each part of the total current. \( I_{ab} \) will not be in absolute value, in order to correctly account for both signs of \( V_{DS} \).

### 4. Extraction procedure

The UMEM is based on the properties of the integral function [20]. In the above threshold regime we have:

\[
H(V_{CS}) = \frac{\int_{0}^{V_{CS}} I_{0} \left( \frac{\gamma}{2} \right) dx}{\int_{0}^{V_{CS}} \left( V_{CS} - V_{T} \right) dx} = \frac{1}{2 + \gamma} \left( V_{CS} - V_{T} \right)
\]

(11)

where parameters \( V_{T}, \gamma_{0}, V_{ab} \) and \( \chi_{a} \) are extracted as indicated in [20], after which the mobility is calculated using (2). The upper limit of integration is the maximum gate voltage up to which the transfer curve in linear regime was measured. When the device is biased up to high voltage values the exact upper limit of integration is given by the \( V_{CS} \) value where the maximum current slope occurs, i.e. the maximum value of transconductance (\( g_{m} \)). With this, series resistance effects influencing the device characteristics at high voltage are avoided which in turn affect the calculation of \( \gamma \) and therefore, the mobility. It is recommended to use the same range of \( V_{CS} \) values for both transfer curves in linear and saturation.

In the above threshold regime, an analytical relation between above threshold model parameters and the characteristics of the distribution of tail states has not been demonstrated yet.

However in the subthreshold regime, the model parameters \( V_{bb}, \gamma_{b} \) depend on the temperature \( T_{2} \) and \( g_{ado} \). The characteristic temperature of the deep states (\( T_{2} \)) and the density of deep states (\( g_{f0} \)) is extracted in a direct and simple way from the experimental measurements [31]. The integral function will be:

\[
H(V_{CS}) = \frac{\int_{0}^{V_{CS}} \left( \frac{\gamma}{2} \right) dx}{\int_{0}^{V_{CS}} \left( V_{CS} - V_{FB} \right) dx} = \frac{1}{2 + \gamma_{b}} \left( V_{CS} - V_{FB} \right)
\]

(12)

where \( V_{FB} \) is obtained from the intercept, and \( 2T_{2}/T \) from the slope of (12) in a region for \( V_{CS} < V_{T} \) but immediately below \( V_{T} \), where \( H \) vs. \( V_{CS} \) shows a linear dependence. This is based in the fact that the variation of the mobility in the subthreshold region corresponds to the strong decay observed as \( V_{CS} \) becomes smaller than \( V_{T} \). When \( V_{CS} \ll V_{T} \) the mobility is very small and it can be considered that it does not depend on \( V_{CS} \).

After extracting \( T_{2} \), we have the density of deep states at Fermi level equal to:

\[
g_{f0} = g_{ado} \cdot \exp \left( \frac{-E_{F} - E_{F0}}{kT_{2}} \right)
\]

(13)

where \( E_{F0} \) is the Fermi level.

So, using the integral method, we manage to extract the values \( T_{2} \) and \( g_{f0} \) using simple mathematics, with no need of graphical methods or non-linear optimization.

### 5. Validation and discussion of the results

In Fig. 2 we present the difference between the experimental measurements (\( I_{DSexp} \)) and the improved model in black (squares) and between the experimental measurements and the model without improvement in red (circles). We can see we have less difference for the model with its output saturation behavior improved.
The difference between the measured current (\(I_{DS,\text{exp}}\)), the model with improvement (\(I_{DS,\text{improved}}\)) and the model without improvement (\(I_{DS,\text{notimproved}}\)) for \(V_{GS} = 8\text{V}\).

**Fig. 2.**

Output characteristics. Model (lines) and measurements (symbols).

**Fig. 3.**

Output conductance characteristics. Model (lines) and measurements (symbols).

**Fig. 4.**

Transfer characteristics. Model (lines) and measurements (symbols).

**Fig. 5.**

Transconductance characteristics. Model (lines) and measurements (symbols).

**Fig. 6.**

Calculated and measured \(g_{m}/I_{DS}\) versus \(I_{DS}\). Model (lines) and measurements (symbols).
by a new asymptotic function, demonstrating that our model brings an important upgrade to previous AOS TFTs models.

Because this difference depends on the geometry of the experimental devices it may be more accentuated for other device technologies.

In Figs. 3–5 we validate our model with measurements for the output and transfer characteristics and also for the output conductance values. It can be seen that in all cases we have a good agreement with the experimental data.

By including the new asymptotic function (Eq. (4)) we will have an improvement visible in the output characteristic (Fig. 3) and in the output conductance figure (Fig. 4). Also, in Fig. 2 we observe that our model correctly reproduces the change of the drain current at the point $V_{DS} = 0$ V, as explained in Section 3.1.1. Hence, we demonstrate the symmetry between source and drain electrodes.

Figs. 5 and 6 will implement a correction factor of $\Delta V_{GS}$ equal to 0.2 V. In Fig. 5 we show the transfer characteristics for two values of $V_{DS}$ while Fig. 6 presents the transconductance $g_m = \frac{\partial I_D}{\partial V_G}$ with a good agreement with the measured data. $g_{ms/2}$ is a relevant function due to its strong relation to the performance of analog circuits [33]. In Fig. 7 it can be seen that our model correctly reproduces the experimental $g_{ms/2}$ curve. We have a low $g_{ms/2}$ which means that we will have a high transit frequency.

In conclusion, the proposed model properly follows the experimental characteristics in all the different regimes of operation of the GIZO TFT, by using only one set of extracted parameters presented in Table 1. The mobility $\mu_{eff}$ is relatively high and consistent with previously reported GIZO mobility values. Its variation with $V_{GS}$ is highlighted in Eq. (2).

6. Conclusions

In this paper we present an advanced compact model for the drain-to-source current of amorphous GIZO TFTs with accurate output asymptotes. The model includes direct parameter extraction methods applied for the first time to GIZO devices. No graphical methods or non-linear optimization are needed to calculate any of the parameters.

For validation, typical experimental characteristics of GIZO TFTs were compared with our model, showing a good agreement. Also, the demonstrated symmetry of the source and drain electrodes is an important plus and opens the way to an extended range of applications such as logic functions. The Verilog-A code of our model has already been successfully implemented in Smart Spice.

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Table 1

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<th>$\gamma_s$</th>
<th>$V_{sat}$</th>
<th>$\lambda$</th>
<th>R</th>
<th>$\mu_{eff}$</th>
<th>$V_{FB}$</th>
<th>$V_{DS}$</th>
<th>$\gamma_m$</th>
<th>$V_{(dec)}$</th>
<th>$T_2$</th>
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<td>$-2.79 \times 10^{-3}$</td>
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References


