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Modelling and extraction procedure for gate insulator and fringing gate capacitance components of an MIS structure

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Abstract

CMOS technology has been guided by the continuous reduction of MOS transistors used to fabricate integrated circuits. Additionally, the use of high-*k* dielectrics as well as a metal gate electrode have promoted the development of nanometric MOS transistors. Under this scenario, the proper modelling of the gate capacitance, with the aim of adequately evaluating the dielectric film thickness, becomes challenging for nanometric metal-insulator-semiconductor (MIS) structures due to the presence of extrinsic fringing capacitance components which affect the total gate capacitance. In this contribution, a complete intrinsic–extrinsic model for gate capacitance under accumulation of an MIS structure, together with an extraction procedure in order to independently determine the different capacitance components, is presented. ATLAS finite element simulation has been used to validate the proposed methodology.

Keywords: extrinsic gate capacitance, capacitance extraction, fringing capacitance, EOT

1. Introduction

The microelectronics industry is based on the use of the well-known MOS structure. In the last few decades, the main concerns related to silicon oxide thinning have been solved by the use of alternative dielectrics with a high dielectric constant (high-*k*), as well as the use of metal gate electrodes, allowing the continuous evolution of the industry [1–5].

An important task related to the dielectric evaluation is the extraction of the equivalent electric thickness. Usually, the physical and SiO_2 equivalent thickness can be obtained from the area normalized accumulation capacitance (C_{acc}), which can be expressed as [6, 7]:

$$C_{acc} = C_i = \frac{k_{ins}\epsilon_0}{t_{ph}} = \frac{k_{ox}\epsilon_0}{EOT} \quad (1)$$

where: C_i is the area normalized insulator gate capacitance, k_{ins} is the insulator dielectric constant, t_{ph} is the physical insulator thickness, k_{ox} is the SiO_2 dielectric constant, *EOT* is the equivalent oxide thickness and ϵ_0 is the electrical permittivity of the vacuum.

Some authors have addressed the issues regarding the quantum-mechanical effects and gate leakage current on C_i [8, 9]. Usually, relatively large area devices are used for dielectric evaluation. However, the use of large area devices becomes challenging for nanometric technologies due to the important increase on the gate current promoted by the ultra-thin dielectric layers and large area devices, the increment on the extrinsic failure probability [10], as well as non-uniformity concerns [11, 12], which hinder proper characterization.

However, as gate length is aggressively reduced, the fringing parasitic gate capacitance starts to affect the capacitance behavior [13]. Those components appear in parallel with the gate electrode, and therefore the total width normalized accumulation gate capacitance becomes:

$$C_{acc}L_g = C_iL_g + C_e \quad (2)$$

where L_g is the metal length and C_e is the total width normalized extrinsic gate capacitance.

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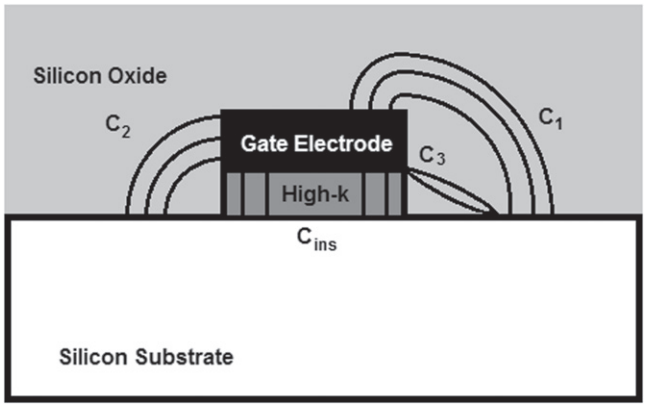
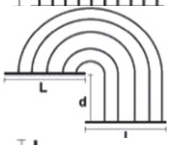
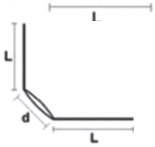


Figure 1. Schematic representation of the cross section of the MIS structure. The intrinsic and extrinsic capacitance components are shown.

Table 1. Basic capacitive structures considered in the model [18].

Structure	Cross section	Equation[a]
Parallel-plate		$C = \frac{k\epsilon_0}{d}L$
Flat-plate non parallel		$C = \frac{k\epsilon_0}{\pi}\ln\left(1+\frac{L}{d}\right)$
Perpendicular-plate		$C = \frac{2k\epsilon_0}{\pi}\ln\left(1+\frac{L}{d}\right)$
Fringing Coupling		$C = \frac{k\epsilon_0}{2\pi}\ln\left(\frac{\pi W}{d}\right)$

[a] L represents the metal length, d represents the distance between metal plates, W represents the metal width and k is the dielectric constant.

The presence of those parasitic components can produce a significant error on the extracted parameters for short MOS capacitors. Therefore, an extraction methodology able to determine, independently, the area normalized gate capacitance, as well as the fringing extrinsic capacitances for standard MOS structures, has been very recently presented [14]. In this contribution, the methodology is extended for a metal-insulator-semiconductor (MIS) structure considering a high-k dielectric material with the aim of properly determining the *EOT* as well as the fringing extrinsic components.

2. Gate capacitance model and extraction procedure

Figure 1 shows the cross section of the MOS structure considered in this analysis. A high-k dielectric material under the metal gate electrode is considered. The surrounding area, defined as a spacer, is covered by SiO_2 with the aim of including the extrinsic components. Four components can be identified [14]. As was explained previously, those components can be represented by simple capacitive structures, as table 1 shows [15–18].

The general model as well as the extraction procedure was presented in [14].

2.1. Intrinsic capacitance

The intrinsic capacitance of an MIS structure corresponds to the gate insulator capacitance ($C_{\rm ins}$) in a parallel plate structure which is bias dependent. Under accumulation condition, the width normalized intrinsic capacitance is defined as:

$$C_{\rm ins} = \frac{k_{\rm ins}\epsilon_0}{t_{\rm ph}}L_g = \frac{k_{\rm ox}\epsilon_0}{EOT}L_g \tag{3}$$

2.2. Parasitic fringing capacitance components

As can be observed in figure 1, three main parasitic components have been considered:

C_1: Represents the electric coupling between the top surface of the gate electrode and the silicon surface. This component corresponds to a flat-plate non-parallel structure, where the plate's length is restricted by $L_g/2$ and the distance between the plates are the addition of the metal and dielectric thicknesses ($t_m + t_{\rm ph}$). Considering table 1, the width normalized capacitance of this component can be expressed as:

$$C_1 = \alpha_1\frac{k_{sp}\epsilon_0}{\pi}ln\left[1+\frac{L_g}{2(t_m+t_{\rm ph})}\right] \tag{4}$$

where α_1 is a fitting parameter and k_{sp} is the dielectric constant of the spacer region.

Considering that $L_g \ll 2(t_m + t_{\rm ph})$, which is a reasonable assumption for nanometric MIS structures and using the first term of the Taylor series expansion for the logarithmic term of equation (4), C_1 can be expressed as:

$$C_1 \cong \alpha_1\frac{k_{sp}\epsilon_0}{\pi}\left[\frac{L_g}{2(t_m+t_{\rm ph})}\right] \tag{5}$$

C_2: Represents the electric coupling between the sidewall of the gate electrode and the silicon surface. It corresponds to a perpendicular plate structure where the plate's length is restricted by the metal thickness and the distance between the plates is related with the dielectric thickness. From table 1, the width normalized C_2 capacitance can be determined using the fitting parameter α_2 as:

$$C_2 = \alpha_2\frac{2\,k_{sp}\epsilon_0}{\pi}ln\left(1+\frac{t_m}{t_{\rm ph}}\right) \tag{6}$$

C_3: Represents the electric coupling between the bottom corner of the metal electrode and the silicon surface as the fringing component indicated in table 1. In this case, the distance between the plates becomes $\sqrt{2}\ t_{\rm ph}$. Thus, the width

normalized C_3 capacitance can be determined by:

$$C_3 = \alpha_3 \frac{k_{sp}\epsilon_0}{2\,\pi} ln\left(\frac{\pi\, W_g}{\sqrt{2}\;\; t_{\rm ph}}\right) \tag{7}$$

where W_g is the metal width. For width normalized capacitance, a value of 1 μm is considered. Therefore, in order to maintain dimensional balance $W_g = 10^{-4}$ cm is used. α_3 is a fitting parameter.

2.3. Total gate capacitance

The fringing components are present at both sides of the MOS structure and appear in parallel with the dielectric capacitance. Hence, the total width normalized gate capacitance (C_g), under accumulation, can be expressed as:

$$C_g = C_{\rm ins} + 2(C_1 + C_2 + C_3) \tag{8}$$

where the total extrinsic capacitance corresponds to the second term: $C_e = 2(C_1 + C_2 + C_3)$.

Substituting equations (3), (5)–(7) in (8) and reordering the terms, C_g can be expressed as:

$$\begin{aligned} C_g = &\left[\frac{k_{\rm ox}\epsilon_0}{EOT} + \alpha_1 \frac{k_{sp}\epsilon_0}{\pi}\frac{1}{(t_m + t_{\rm ph})}\right] L_g \\ &+ \alpha_2 \frac{4\, k_{sp}\epsilon_0}{\pi} ln\left(1 + \frac{t_m}{t_{\rm ph}}\right) \\ &+ \alpha_3 \frac{k_{sp}\epsilon_0}{\pi} ln\left(\frac{\pi\, W_g}{\sqrt{2}\;\; t_{\rm ph}}\right) \end{aligned} \tag{9}$$

Equation (9) represents the general model for a nanometric MIS structure, which includes the extrinsic components.

2.4. Capacitance components extraction procedure

As can be observed, equation (9) follows a linear dependence with respect to the gate electrode length. The slope (m) and the y-axis intercept (B) are defined as:

$$m = \frac{k_{\rm ox}\epsilon_0}{EOT} + \alpha_1 \frac{k_{sp}\epsilon_0}{\pi}\frac{1}{(t_m + t_{\rm ph})} \tag{10}$$

$$B = \alpha_2 \frac{4\, k_{sp}\epsilon_0}{\pi} ln\left(1 + \frac{t_m}{t_{\rm ph}}\right) + \alpha_3 \frac{k_{sp}\epsilon_0}{\pi} ln\left(\frac{\pi\, W_g}{\sqrt{2}\;\; t_{\rm ph}}\right) \tag{11}$$

In equation (10), m shows a linear function with respect to the term $1/(t_m + t_{\rm ph})$. Considering that $t_m \gg t_{\rm ph}$, the slope (m_2) and the intercept (B_2) of this linear function, correspond to:

$$m_2 = \alpha_1 \frac{k_{sp}\epsilon_0}{\pi} \tag{12}$$

$$B_2 = \frac{k_{\rm ox}\epsilon_0}{EOT} \tag{13}$$

Thus, the α_1 fitting parameter as well as intrinsic area normalized gate dielectric capacitance are obtained from (12) and (13), by obtaining the corresponding slope and the y-axis intercept of (10).

It is worth noticing that B_2 allows us to determine the area normalized gate capacitance without the parasitic components. Hence, EOT or $k_{\rm ins}$ can be obtained from this value.

Additionally, the derivative of B with respect to t_m is expressed as:

$$\frac{d}{dt_m}(B) = \alpha_2 \frac{4\, k_{sp}\epsilon_0}{\pi}\left(\frac{1}{t_m + t_{\rm ph}}\right) \tag{14}$$

Equation (14) also exhibits a linear dependence with respect to $1/(t_m + t_{\rm ph})$, where the slope (m_3) corresponds to:

$$m_3 = \alpha_2 \frac{4\, k_{sp}\epsilon_0}{\pi} \tag{15}$$

Therefore, α_2 is determined from equation (15). Finally, α_3 can be obtained by subtracting the C_2 component from equation (11) for a desired gate electrode thickness value.

Hence, the proposed extraction procedure allows us to determine, independently, the intrinsic normalized dielectric capacitance as well as the parasitic components.

3. Simulations

Two sets of 2D ATLAS simulations were performed in order to verify the ability of the method to properly determine the capacitance components. Both groups of simulations considered high-k dielectric material as the insulator; the metal length was varied from 10–60 nm and the metal thickness was varied from 50–100 nm. The first group considered a fixed physical dielectric thickness of 5 nm and different values of k from 13–23. The second group considered a fixed EOT of 0.7 nm and k from 13–23.

The MIS structure was enclosed by silicon oxide as a spacer. Due to the symmetry, half of the MIS structure was used in the simulations with the aim of allowing us to define a mesh closed enough to properly simulate the extrinsic components. Figure 2 shows the MIS structure used in the ATLAS simulations and the main technological parameters.

4. Results

The new extraction procedure has been applied to both sets of simulations with the aim of determining the intrinsic and extrinsic gate capacitance, as well as the corresponding EOT. Tables 2 and 3 summarize the extracted parameters using the proposed method for SiO_2 as a spacer.

Figure 3 shows the comparison of the simulated and the modeled C_g versus L_g for the first group of the simulation. The metal thickness is fixed to 50 nm. The modeled results were obtained using (9) and the values for α_1, α_2 and α_3 are

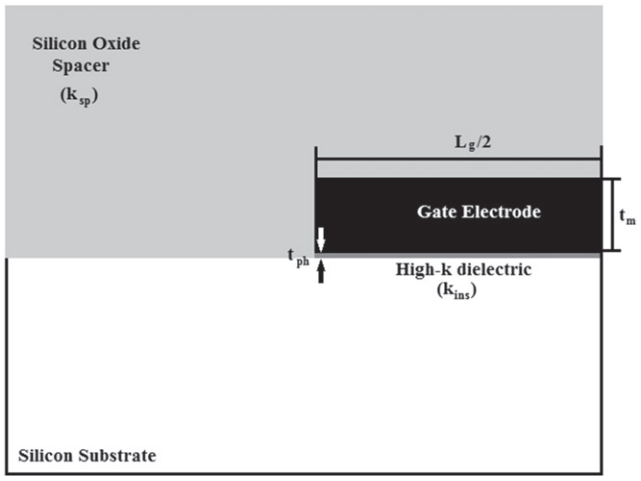


Figure 2. Schematic representation of the structure used in the simulations, where the main technological parameters are shown.

Table 2. Summary of the extracted parameters for the first simulation group.

Dielectric constant	*EOT*	α_1	α_2	α_3
13	1.5	1.3	1.08	0.73
16	1.2	1.3	1.08	0.73
18	1.08	1.3	1.08	0.74
20	0.97	1.3	1.08	0.74
23	0.85	1.3	1.08	0.74

Table 3. Summary of the extracted parameters for the second simulation group.

Dielectric constant	*EOT*	α_1	α_2	α_3
13	0.7	1.3	1.0	0.77
16	0.69	1.3	1.0	0.7
18	0.69	1.3	1.1	0.7
20	0.69	1.4	1.0	0.8
23	0.7	1.4	1.1	0.7

shown in table 2. As can be observed, the model and extraction procedure presented allows us to accurately reproduce the capacitance values obtained by simulation.

Figure 4 shows the comparison of the total gate capacitance and the insulator capacitance versus metal length for SiO_2 and Si_3N_4 as spacer material. As can be seen, the increment of the spacer dielectric constant will increase the impact of the extrinsic gate capacitance as indicated by equations (4)–(7). Additionally, this plot shows that the insulator capacitance is overestimated if the parasitic components are not considered in the MIS structure evaluation. Thus, the parameters extracted from the accumulation capacitance will suffer substantial deviation from their real values.

Figures 5(a) and (b) show the comparison of the extracted *EOT* using the new procedure and the traditional one (EOT_{trad}) determined as $EOT_{trad} = k_{ox}.\varepsilon_0.L_g/C_{sim}$ where C_{sim} corresponds to the width normalized accumulation capacitance obtained from 2D simulations. This is done for

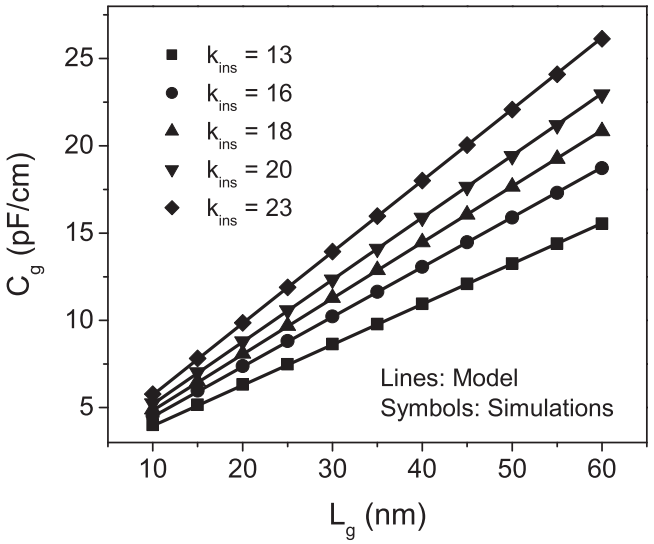


Figure 3. Comparison of the simulated and modeled gate capacitance versus metal length for several dielectric constant values. A metal thickness of 50 nm and SiO_2 as spacer material are used.

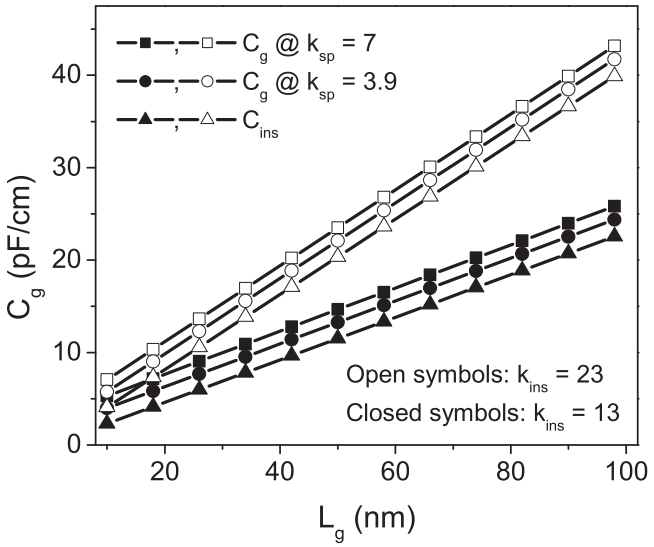


Figure 4. Modeled total capacitance and insulator capacitance versus metal length for high-*k* dielectric with $k = 13$ and 23, SiO_2 and Si_3N_4 as spacer material are shown. t_m and t_{ph} with values of 50 and 5 nm, respectively, are used.

each simulation group versus the dielectric constant of the MIS structure. For comparison, the value used in the simulations determined as $EOT_{sim} = (k_{ox}/k_{ins}).t_{ph}$, is presented.

As can be seen, the traditional extraction procedure induces an important error on the *EOT* determination. Such an error increases as the metal length is reduced and an overall difference between 25%–40% is observed. The difference between the real and the extracted values is related to the parasitic capacitance, as was explained before. On the other hand, because the new method discriminates the extrinsic capacitance components, it allows us to recover the accuracy on the *EOT* extraction.

Figure 6(a) shows the comparison of the EOT_{trad} and the corresponding *EOT* used in the simulations (EOT_{sim}) versus

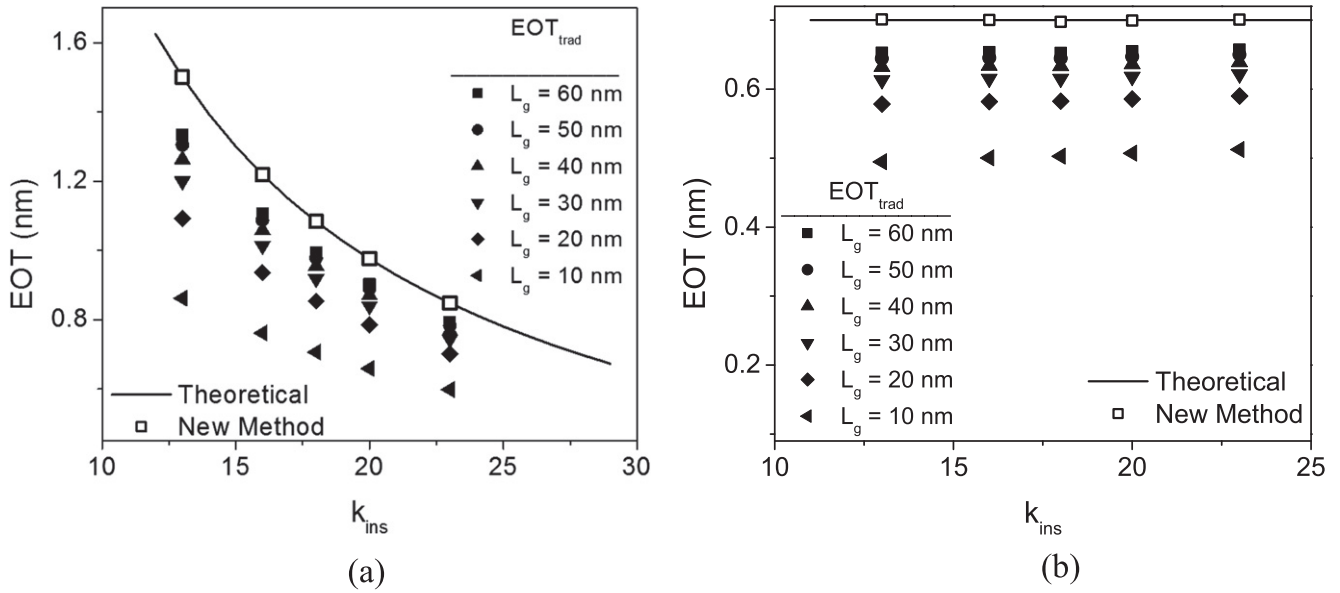


Figure 5. Comparison of the extracted *EOT* versus insulator dielectric constant for (a) the first and (b) the second group of simulations. A metal thickness of 50 nm and SiO_2 as the spacer material are used.

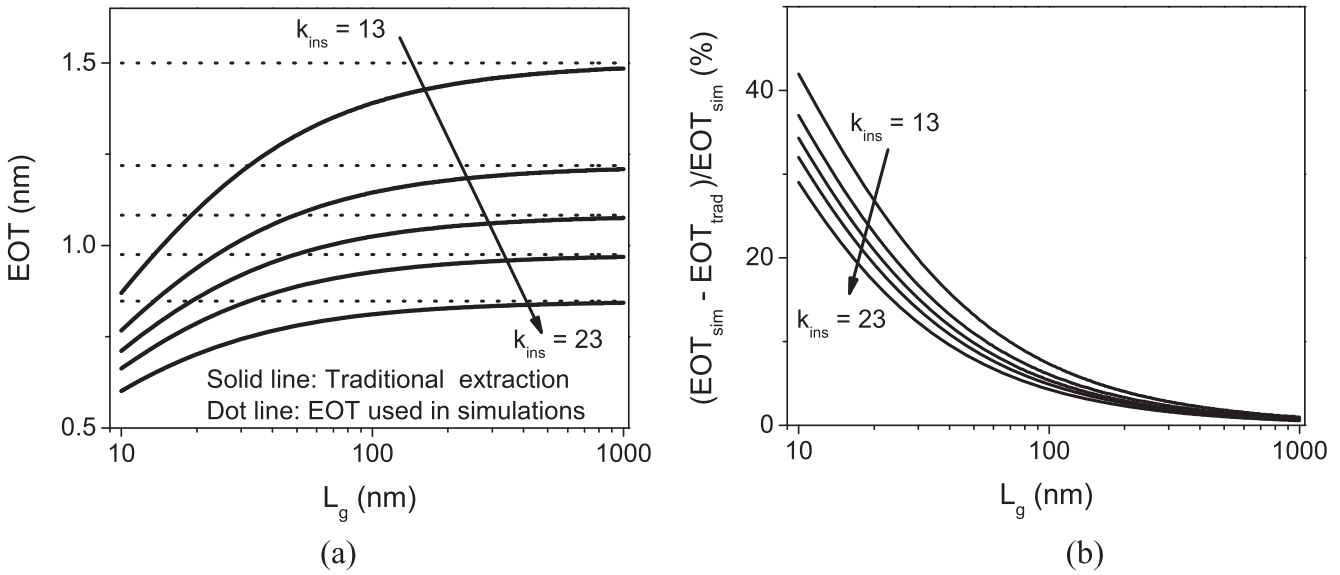


Figure 6. Comparison of EOT_{trad} and the error versus L_g for the first group of simulations. A metal thickness of 50 nm and SiO_2 as spacer material are used.

L_g, for the first group of simulations, while figure 6(b) shows the error on the extracted value. Additionally, figures 7(a) and (b) show, respectively, the comparison of EOT_{trad} versus L_g and the error for the second group of simulations. As can be observed, for extremely short devices, the error produced by the traditional extraction procedure is very high. It is worth noticing that the error is reduced as the dielectric constant of the high-k material is increased. Additionally, for devices with L_g larger than ~150 nm the error becomes smaller than 5%.

Figure 8 shows the comparison of the error versus L_g when two different spacer materials are considered. As shown, the error on the traditional *EOT* extraction increases as the spacer dielectric constant is increased as a consequence of the increment on C_e components. Hence, for Si_3N_4 spacers, the error becomes smaller than 5% for L_g greater than ~300 nm.

Figure 9 shows the comparison of the total width normalized extrinsic capacitance (C_e) versus L_g for different metal thickness.

As t_m is increased, C_e grows due to the increment of the C_2 component as indicated by (6). It is worth noticing that the C_1 component is reduced with the increment on t_m as (5) indicates. However, because its value is very small with respect to C_2 [14], it has an insignificant impact on the C_e dependence with t_m. Under this scenario, the reduction of the gate electrode thickness can be considered in order to reduce the impact of the parasitic capacitances on the overall MIS structure behavior.

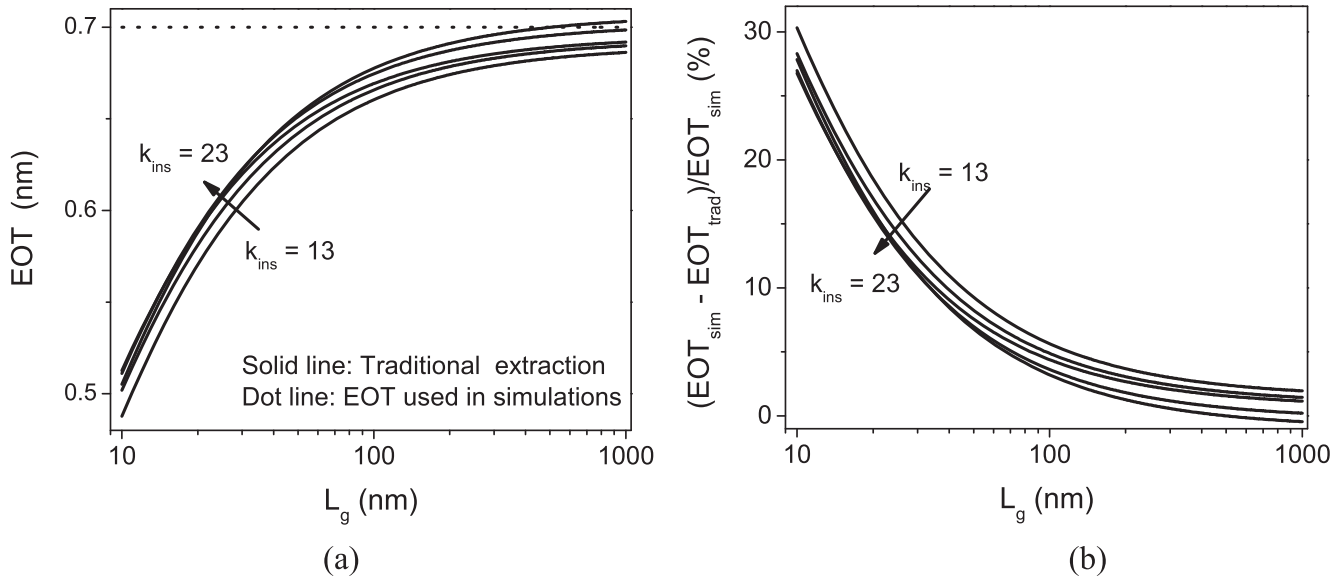


Figure 7. Comparison of EOT_{trad} and the error versus L_g for the second group of simulations. A metal thickness of 50 nm and SiO_2 as spacer material are used.

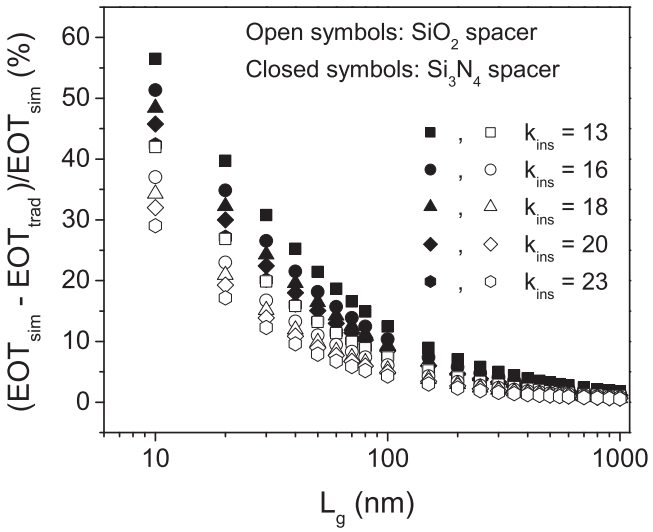


Figure 8. Comparison of traditional *EOT* extraction error versus L_g for SiO_2 and Si_3N_4 as spacer material. t_m and t_{ph} with values of 50 and 5 nm, respectively, are used.

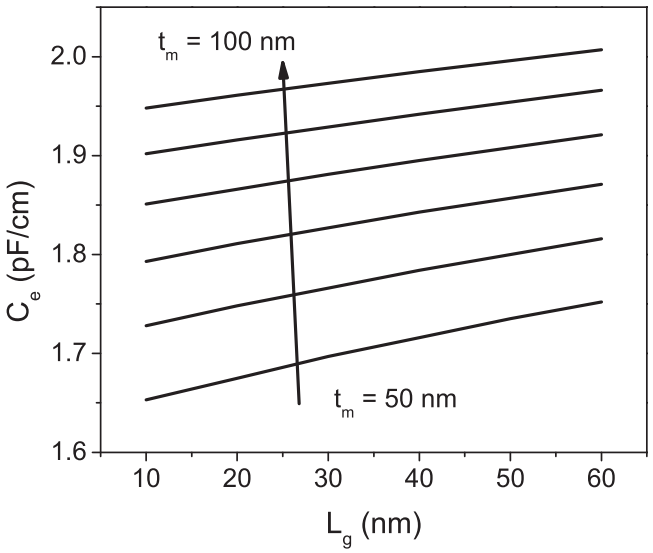


Figure 9. Total extrinsic capacitance versus metal length for different metal thickness. A physical dielectric thickness of 5 nm and SiO_2 as spacer material are used.

5. Conclusions

A full model able to properly reproduce the full intrinsic and extrinsic gate capacitance for nanometric MOS structures with high-*k* dielectric material has been presented. This model considers the presence of the intrinsic capacitance component as well as the presence of three different parasitic components. Furthermore, an extraction procedure with the aim of independently determining the four capacitance components has been developed.

The overall results indicate that the presence of the parasitic capacitance produces an error on the *EOT* determination of about 25%–40% when they are neglected. However, the extraction procedure here proposed allows us to accurately determine the *EOT*, even for nanometric MOS structures. Furthermore, as the dielectric constant of the gate dielectric increases, the error on the extracted value is reduced due to the increased intrinsic capacitance. Finally, the model and extraction procedure allows us to determine independently the three extrinsic capacitance components.

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Aplicación en Fisiología y Optoelectrónica' and by CONACyT Projects 237213 and 236887.

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