Charge-based compact analytical model for triple-gate junctionless nanowire transistors

F. Ávila-Herrera a,*, B.C. Paz b, A. Cerdeira a, M. Estrada a, M.A. Pavanello b

a Sección de Electrónica de Estado Sólido, Depto. Ingeniería Eléctrica, CINVESTAV-IPN, Ciudad de México 07360, Mexico
b Department of Electrical Engineering, Centro Universitario da FEI, Av. Humberto de Alencar Castelo Branco n. 3972, 09850-901, São Bernardo do Campo, Brazil

1. Introduction

The search of MOSFETs structures that allow greater control of the electrical characteristics and thus reduce the undesired effects coming from the miniaturization has led to the appearance of the first tridimensional transistor in 1999, the FinFET [1]. This device was introduced into volume production by the electronics industry [2], presenting technological compatibility with the self-aligned process steps and planar technology. Currently, the studies are being focused on the multiple gate structures as double and triple gate. The efforts are not only invested on inversion mode (IM) being focused on the multiple gate structures as double and triple process steps and planar technology. Currently, the studies are only 8 adjusting parameters.

A new compact analytical model for short channel triple gate junctionless transistors is proposed. Based on a previous model for double-gate transistors which neglected the fin height effects, a new 3-D continuous model has been developed, including the dependence of the fin height and the short channel effects. An expression for threshold voltage is presented. The model defines a one-dimensional semiconductor effective capacitance due to the width and the height of the fin, which in turn redifines the potentials and charges, without altering the general modeling procedure. Threshold voltage roll-off, subthreshold slope, DIBL and channel length modulation, as well as, the mobility degradation and the velocity saturation have been introduced into the model. The validation was done by 3-D numerical simulations for different fin heights and channel lengths, as well as, by experimental measurements in nanowire transistors with doping concentrations of $5 \times 10^{18}$ and $1 \times 10^{19}$ cm$^{-3}$. The developed model is suitable for describing the current–voltage characteristics in all operating regions from double-gate to nanowire transistor with only 8 adjusting parameters.

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have been developed for double gate JLT devices (DGJLT), [7–10], models for triple gate JLT (TGJLT) are very scarce [11,12]. Besides, two models for describing the operation of both devices are commonly used.

A short channel DGJLT for compact modeling was already presented in [13]. In this context, an extension of this model was developed for TGJLT, also considering the short channel effects [14,15], which due to its tridimensional physical description, can be used for modeling DG and TG structures and nanowire transistors without the need of switching models [12]. In this work, we present in detail, this generalized model. The influence of the fin height ($H_{fin}$) and its width ($W_{fin}$) are taken into account in the calculation of the capacitance included in the expression of the current and of the $V_f$. Among main short channel effects (SCE), it considers velocity saturation, mobility degradation, threshold voltage roll-off, DIBL, subthreshold slope and channel length modulation. The model also includes the series resistance. The expression for current is continuous in all operation regimes, without using approximations for the transition between the two methods of conduction [11,12].

Although models for triple-gate transistors have been developed before, [11,12,16], most of them use approximations for carriers in the Poisson's equation, adjustable transitions points and considering complete ionization by Boltzmann statistic even for high doping concentrations. Now in this paper it is developed a new physically based model to describe the influence of geometrical parameters considering for first time their dependences on the capacitances obtaining a complete analytical continuous model for all operation regimes, also including the incomplete ionization due to the Fermi statistic and valid from nanowires to double gate JLT and presenting an explicit expression for the threshold voltage.

The validation of the model is supported by both 3-D numerical simulations and by experimental measurements of devices with different fin height, width, channel length and doping concentration.

2. Tridimensional core model description

In order to introduce in the model the effects induced by the reduction of $H_{fin}$ in a tridimensional structure as the one presented in Fig. 1a, from now on we will use the subscript “L” to represent parameters already including such dependence.

The studied device is shown in Fig. 1a, while its cross section is shown in Fig. 1b. As can be seen, in tridimensional devices the height of the transistor plays an important role in the semiconductor through another capacitance, $C_{gfin}$ related to the height of the fin, in parallel with the 2-D capacitance caused by the silicon width, $C_t$. The total equivalent silicon capacitance per unit length, $C_{eq}$, is now obtained as:

$$C_{eq} = C_t \cdot H_{fin} + C_{gfin} \cdot W_{fin} = \frac{\varepsilon_0}{W_{fin}} \cdot H_{fin} + \frac{\varepsilon_0}{H_{fin}} \cdot W_{fin}.$$  (1)

where $\varepsilon_0$ is the semiconductor permittivity.

We will analyze two possible cases due to the value of $H_{fin}$: (a) when $H_{fin}$ is reduced sufficiently, the value of $C_{gfin}$ increases becoming comparable to $C_t$, this is the case of the nanowire transistor; (b) on the contrary, if $H_{fin}$ increases, the total capacitance tends to the fixed value of the 2-D capacitance, which is the case of a DGJLT.

Using the device symmetry, the analysis is done in one half of the structure, considering the effective channel width as $W_{eff} = H_{fin} + W_{fin}/2$ for TGJLT or as $W_{eff} = H_{fin}$ for DGJLT. The new effective gate capacitance per unit length including both, the lateral and top sides of the fin $C_{tot}$ is now defined as:

$$C_{tot} = \frac{\varepsilon_0}{W_{eff}} \cdot W_{fin} = C_{eq} \cdot W_{eff},$$

where $\varepsilon_0$ is the dielectric permittivity; $t_{ox}$ is the equivalent oxide thickness, EOT, and $C_{tot}$ is the gate capacitance per unit area.

2.1. Model for the potentials

After obtaining the total effective silicon capacitance $C_{eq}$ and considering the effective channel width $W_{eff}$ already defined, the same expressions for the potentials previously obtained for the DG device can be used [17].

The density of charges is equal to:

$$\rho = qN_d \left(1 - e^{\frac{\varphi}{kT}}\right).$$

The expression for the surface electric field, $E_{sd}$, is now rewritten as:

$$E_{sd} = \varphi L \frac{\varepsilon_{ox}}{C_{tot}} \beta \text{sign}(\varphi_L) \sqrt{e^{\frac{\varphi}{kT}} - \xi_L \cdot \varphi_L - 1},$$

where $\beta = \sqrt{\frac{2\varphi_L}{C_{tot}}} \xi_L = \left(1 - \frac{1}{\eta_{sc}}\right)$ and $\eta_{sc} = \frac{\varphi_S W_{fin}}{C_{tot} \varphi_L}$, $\varphi_S = kT/q$ is the thermal potential; $q$ is the electron charge; $\varphi$ is the potential at the channel and $V$ is the potential drop across the channel, from source $V_S = 0$ to drain $V_D$, $q\eta_{sc}$ is the total normalized fixed charge in the semiconductor; $\varphi_L$ that is the normalized difference of potentials between the surface, $\varphi_S$, and the center, $\varphi_L$, with respect to $\varphi_S$, calculated as:

$$\varphi_L = \varphi_{sat} + LW \left[-\varphi_{sat}e^{-\frac{\varphi - \varphi_S}{kT}}\right],$$

where $\varphi_{sat}$ is the value of the potential difference at deep subthreshold [17]. $W_L$ is the Lambert function implemented and used before in [18].

Applying the Gauss’s law the relation between $\varphi_{sat}$ and the applied voltages is obtained by:

$$V_C - V_{fin} = \varphi_{sat} + \text{sign}(\varphi_L) \varphi_L \sqrt{e^{\frac{\varphi + \varphi_S}{kT}} - \xi_L \cdot \varphi_L} - 1,$$

This expression does not have an analytical solution, however, a third order precise solution based on the Newton–Raphson’s method was developed and implemented in [13].

2.2. Continuous charge model

The new total and the mobile charge, $q_{tot}$ and $q_{sat}$, can be expressed similarly as for the DG structure, only using the parameters that include the effects of the fin height, as follows:

$$q_{tot} = -\text{sign}(\varphi_L) \varphi_L \sqrt{e^{\frac{\varphi_{sat} + \varphi_S}{kT}} - \xi_L \cdot \varphi_L} - 1,$$

$$q_{sat} = q_{tot} - \frac{\varphi_{sat}}{2}.$$
As will be shown, the above expressions allow calculating the charge in all the operation regimes, continuously, which is something not always possible with most of the JLT triple gate models previously reported [11,12].

As we used in the case of the DG structures to obtain the current expression, it is necessary to decouple the charge in expression (7) for each operation regime. Following the same procedure as in [17]:

$$q_{\text{depl}} = \beta_L \sqrt{\epsilon N_D \zeta_L - \zeta_L \cdot \zeta_L - 1 - q_{\text{depl}}/2}$$  \hspace{1cm} (9)

$$q_{\text{depl}} = -\beta_L \sqrt{\epsilon N_D \zeta_L - \epsilon N_D \zeta_L - 1 - q_{\text{depl}}/2}$$  \hspace{1cm} (10)

It should be noted that the charge expressions in depletion (9) and in accumulation (10) only depend on one variable and are used for solving analytically the integral of the drain current. All the calculations are performed using the continuous expression for the charge in order to reduce the error.

2.3. Threshold voltage

The expression for the long channel $V_T$ of the triple gate structure, in which the effects of the $H_{\text{Fin}}$ variation are included, is calculated also by the maximum of second derivative of the potential for DGJLT devices as in [19], but integrating now the new capacitances obtained for the triple gate structure. The new expression obtained is:

$$V_{\text{TL}} = V_{\text{FB}} - \varphi_s \left(\frac{q_{\text{depl}}}{2} - \frac{1}{4} - \zeta_{\text{TL}} - \ln \left(\frac{1 - \zeta_{\text{TL}}}{\zeta_{\text{TL}}/2}\right)\right).$$  \hspace{1cm} (11)

where the normalized difference of potentials at the threshold voltage is equal to:

$$\zeta_{\text{TL}} = \frac{\zeta_{\text{TL}}}{1 - \zeta_{\text{TL}}} \left[1 - \zeta_{\text{TL}} \left(\frac{1}{2 \zeta_{\text{TL}}/2}\right)^2\right].$$  \hspace{1cm} (12)

It is important to remark that the obtained expression [11] for the threshold voltage is valid for structures starting from DG (tall silicon height) down to TG nanowire transistors.

3. Short channel effects

The main short channel effects are more relevant in the subthreshold regime, altering the threshold voltage, the subthreshold slope (S) and the drain induced barrier lowering (DIBL). These effects are incorporated in the model analyzing the behavior of the minimum of potential inside the channel. The channel length modulation is introduced in the model as indicated below.

3.1. Subthreshold characteristic: threshold voltage roll-off, DIBL and subthreshold slope

In subthreshold regime, the 3-D Poisson’s equation can be approached as:

$$\nabla^2 \varphi(x,y,z) = -\frac{\epsilon}{\epsilon_s} \left(\frac{d^2 \varphi}{dx^2} + \frac{d^2 \varphi}{dy^2} + \frac{d^2 \varphi}{dz^2}\right) = -\frac{qN_D}{\epsilon_s}$$  \hspace{1cm} (13)

A solution of the 3-D potential can be obtained applying the superposition method, solving the Poisson's equation for 2-D devices and adding the solution of the 3-D Laplace's equation for 3-D devices. For calculating the minimum of the potential inside the channel, we use the approach for DGJLT presented in [19], where it was assumed a parabolic approximation of the potential (Young approximation) in a fully depleted device and it was found a 2-D natural length, $t_{n,2D}$. For TGLJT, the natural length is corrected considering the additional variation in the electrostatic potential due to the fin height, $\epsilon_{\text{Fin}}$. This dependence is expressed as [20]:

$$t_{n,3D} = \frac{\epsilon_{\text{Fin}}}{4\epsilon_{\text{ox}}} \left(1 + \frac{\epsilon_{\text{ox}} H_{\text{Fin}}}{2\epsilon_{\text{Fin}} t_{\text{Fin}}} \right) H_{\text{Fin}} t_{\text{Fin}}.$$  \hspace{1cm} (14)

while the fin sides field penetration is:

$$t_{n,2D} = \frac{\epsilon_{\text{Fin}}}{2\epsilon_{\text{ox}}} \left(1 + \frac{\epsilon_{\text{ox}} W_{\text{Fin}}}{4\epsilon_{\text{Fin}} t_{\text{Fin}}} \right) W_{\text{Fin}} t_{\text{Fin}}.$$  \hspace{1cm} (15)

An effective natural length can then be defined as the average of $t_{n,2D}$ and $t_{n,3D}$ as [21]:

$$t_{n,\text{eff}} = \frac{1}{A(t_n^{2D} + 1/(2t_{n,3D})^2)}$$  \hspace{1cm} (16)

The minimum of potential at the center is given by [13]:

$$\varphi_{\text{min}} = \left(-\left(U_{\text{eff}}^2 + U_{\text{eff}}^2\right) + 2U_{\text{eff}} U_{\text{D}} \cot\left(L/t_{\text{eff}}\right)\right) + \varphi_{\text{qpt}}.$$  \hspace{1cm} (17)

where $U_{\text{eff}} = V_{\text{Bias}} - \varphi_{\text{qpt}}$, $\varphi_{\text{qpt}} = V_{\text{G}} - V_{\text{FB}} + \frac{2}{\epsilon_{\text{Fin}}} \zeta_{\text{Tg}}$, is the subthreshold potential at the center for a long channel TGLJT device and $V_{\text{Bias}}$ is the built-in voltage at source/drain.

As the channel length reduces enough, an additional effect of the source/drain regions has to be considered. In [8,13], this was done defining an effective built-in potential as:

$$V_{\text{eff}} = V_{\text{G}} + \varphi_{\text{qpt}} - \frac{2}{\epsilon_{\text{Fin}}} t_{\text{eff}}^2 (1 - 1/(1 + \zeta_{\text{Tg}} (V_{\text{bias}} + V_{\text{D}} - \varphi_{\text{qpt}}))) + \frac{qN_D}{\epsilon_{\text{Fin}}} t_{\text{eff}}^2.$$  \hspace{1cm} (18)

The SCE present mainly at subthreshold regime, such as threshold voltage roll-off, subthreshold slope and DIBL are included calculating an effective gate voltage through the increase of the minimum of potential, as follows:

$$V_{\text{eff}} = V_{\text{G}} + \varphi_{\text{qpt}} + \Delta p_s$$  \hspace{1cm} (19)

where $\Delta p_s = \zeta_{\text{Tg}} \varphi_s + qN_D t_{\text{eff}}^2 / \epsilon_{\text{Fin}} \beta_{\text{Tg}} \zeta_{\text{Tg}} - 1$ is the long channel deep subthreshold potential shift observed as $H_{\text{Fin}}$ is reduced, obtained from the difference between the potential calculated by (6) and by the Young approximation [22].

3.2. Channel length modulation

The reduction of the channel length due to the applied drain voltage occurs as a result of the depletion region formed between the channel and the drain terminal, which decreases the channel length in a value of $\Delta L$. This reduction just takes place when $V_D > V_{\text{Dratt}}$, increasing the current by a rate of:

$$\Delta L = \zeta_{\text{Tg}} \sqrt{\frac{2}{q} \frac{V_D - V_{\text{Dratt}}}{qN_D}}.$$  \hspace{1cm} (20)

where $\zeta$ is an adjusting parameter and $V_{\text{Dratt}}$ is the effective drain voltage.

4. Velocity saturation: drain saturation voltage

A typical definition of the drain saturation voltage for long channel devices can be found in [19]. For short channel transistors, the drain saturation voltage is reached, when the electric field makes carriers move at maximum velocity.
In the TGJLT model presented, the drain saturation voltage for long channel devices is calculated as [19]:

\[ V_{\text{Dsat}} = V_D - V_N. \]  

(21)

For short channel devices, the following semi-empirical equation is used to consider the effect introduced by the saturation velocity [13]:

\[ V_{\text{Dsat}} = 0.08 + \eta(V_D - V_N)^{0.33} \]  

(22)

where \( \eta \) is an adjusting parameter and \( V_{\text{sat}} \) is the velocity saturation. The drain saturation voltage is the smaller of the values obtained for \( V_{\text{Dsat}} \) using (21) and (22).

In order to provide a one piece expression without discontinuities, the effective drain voltage, \( V_{\text{Deff}} \), is calculated as follows:

\[ V_{\text{Deff}} = V_{\text{Dsat}} + \frac{1}{2} \left[ V_D - V_{\text{Dsat}} + \varphi_1 - \sqrt{(V_D - V_{\text{Dsat}} + \varphi_1)^2 + 4 \varphi_1 V_{\text{Dsat}}^2} \right]. \]  

(23)

Considering that in subthreshold regime the applied drain voltage, \( V_D \), plays the most important role, the final effective drain voltage, \( V_{\text{Deff}} \), is equal to:

\[ V_{\text{Deff}} = V_D \left[ 1 - \tanh(15(V_D - V_N)) \right] + V_{\text{Deff}} \left[ 1 + \tanh(15(V_D - V_N)) \right]. \]  

(24)

5. Mobility degradation

JLT devices present two types of current depending on the device operation regime. When the device works in depletion regime, the carriers flow through the center of the silicon bar with low field bulk mobility, \( \mu_0 \) [23], not affected by the perpendicular field. In the accumulation regime, an additional current is present at the Si/SiO\(_2\) interfaces due to the accumulated carriers. As the applied voltages increases, the surface collisions of the carriers also increase, causing a reduction of the mobility, limited by the surface roughness scattering.

To consider these effects, the model includes the following expression for the surface mobility [24]:

\[ \mu_x = \frac{\mu_0}{1 + \left[ \theta_1(V_D - V_{FB}) + \theta_2 V_{\text{Deff}} \right] \frac{1}{2} \left[ 1 + \tanh(1.2(V_D - V_{FB})) \right]}. \]  

(25)

where \( \theta_1 \) and \( \theta_2 \) are adjusting parameters for the accumulation current.

6. Series resistance

In real fabricated transistors the channel is always in series with two resistances associated to the source and drain extensions, metal contacts, etc. Fig. 1 shows the drain/source extensions with length \( L_{\text{tot}} \), with a drop voltage defined by Ohm’s law. The total series resistances \( R \) must be taken into account, because it reduces the drain current at high gate voltage. Its incorporation to the model is performed by introducing the following factor [13]:

\[ K_{\text{f}} = \frac{1}{(1 - \frac{V_D}{V_{FB}})} \cdot \frac{K_{\text{f}}}{1 + K_R(V_D - V_N - n V_{\text{Deff}})^{2}\left[ 1 + \tanh(2(V_D - V_N - n V_{\text{Deff}})) \right]^3}, \]  

(27)

where \( K_{\text{f}} = 2 \frac{C_{\text{ox}} W_{\text{eff}}}{L_{\text{tot}}} \mu_{\text{eff}} \) is the current factor and \( n \) is an adjusting parameter.

7. Drain current model

The expression for the drain current is found by solving the integral of the mobile charge:

\[ I_D = K_K \int_{V_s}^{V_D} q_D dV \]  

(28)

The method consists of separating the integral for each operation regime to obtain the current in depletion, \( I_{\text{d}} \), and in accumulation, \( I_{\text{a}} \). Because of paper length, details description of the procedure is found in [17].

7.1. Full and partial depletion current

Integrating (28), a new subthreshold current is calculated by:

\[ I_{\text{d}} = K_{\text{f}} \left[ \int_{V_s}^{V_D} q_D dV \right] \]  

(29)

where

\[ S_a(x) = -2 \cdot \left[ \sqrt{-1 - x} - |\sqrt{1 - x_{\text{SLD}}} \cdot \arctan \left( \frac{-\sqrt{x} - \sqrt{x_{\text{SLD}}}}{\sqrt{1 - x}} \right) \right]. \]  

(30)

evaluating for \( x = \xi_L \cdot \xi_{\text{SLD}} \). With \( x_{\text{SLD}} = \xi_L \cdot \xi_{\text{SLD}} \).

In above threshold regime (partially depleted operation), the current is obtained as:

\[ I_{\text{d}} = K_{\text{f}} \left[ \int_{V_s}^{V_D} q_D dV \right] \]  

(31)

In short channel devices the longitudinal field is stronger, producing a reduction of the effective mobility, \( \mu_{\text{eff}} \), due to majority carriers reaching the saturation velocity. This effect of mobility reduction is described as [25]:

\[ \mu_{\text{eff}} = \frac{\mu_x}{\sqrt{1 + \left( \frac{\mu_{\text{sat}} V_{\text{sat}}}{V_{\text{sat}}} \right)^2}}. \]  

(26)

where the value of \( \mu_{\text{sat}} \) is considered an adjusting parameter.
7.2. Accumulation current

Integrating (28), the current in accumulation regime is obtained as:

\[
I_{acc} = K_K \frac{q}{2} \left[ \frac{1}{\beta_2} \left( V_D - V_S \right) + \frac{1}{\beta_1} \left( V_G - V_{FB} - V_{TB} \right) \right] \\
+ \frac{q}{2} \left[ V_G - V_{FB} - V_{TB} \right] \left[ 1 - \tanh \left( 2 \left( V_G - V_{FB} - V_{TB} \right) \right) \right] \tag{33}
\]

where function \( SaP \) is defined as in [17].

7.3. Total drain current

The total current is as:

\[
I_{tot} = I_{dep} \left[ \frac{1}{2} \left( 1 - \tanh \left( 2 \left( V_G - V_{TB} \right) \right) \right) \right] \\
+ I_{acc} \left[ \frac{1}{2} \left( 1 + \tanh \left( 2 \left( V_G - V_{TB} \right) \right) \right) \right]. \tag{34}
\]

The total drain current in (34) used in this compact model for TGJLT considers the effective gate voltage, effective drain voltage, velocity saturation, mobility degradation and the main SCE previously defined. It is also important to remark that this 3-D current model for TGJLT reduces to the previously developed 2-D model for DGJLT devices, when considering a thick top oxide.

8. Model validation

To validate the developed 3-D model, it was compared with 3-D numerical simulations and also with measurements from devices fabricated at CEA-LETI [26].

The model requires three parameters: \( \mu_0, R \), and \( n \) corresponding to the core model parameters, necessary for long channel transistors. For short channel devices parameters \( \theta_1, \theta_2 \), and \( \lambda \) must be added. The parameters \( \eta \) and \( v_{sat} \) present an almost constant behavior and the extraction can be omitted.

Parameters were extracted in the following sequence: \( \mu_0 \) from the maximum linear \( g_m \) [26], \( \theta_1 \) and \( \theta_2 \) from the accumulation current in the linear and saturation characteristics [13], \( R \) from the attenuation of the linear characteristic and \( n \) from the saturation characteristic [19] and \( \lambda \) from the output characteristic at saturation [13]; \( \eta \) is obtained from the output characteristic [13] with a constant value equal to 0.13. \( v_{sat} \) was fixed to \( 1.2 \times 10^5 \) cm/s.

8.1. Simulations results and discussion

The validation of the presented analytical compact model was done using 3-D ATLAS simulations [27]. The simulated structure is in Fig. 1. CVT mobility model was used, considering the bandgap narrowing variation with doping concentration dependence as the Slotboom model, as well as the affinity variation, impact ionization and carrier velocity saturation effect. Simulations were performed introducing the following parameters into the simulator: metal gate work-function of 5.2 eV; positive interface charge \( N_s = 5 \times 10^{10} \) cm\(^{-2}\); N-type doping concentration, \( N_D = 5 \times 10^{18} \) cm\(^{-3}\); lateral and top oxide, \( t_{ox} = t_{extox} = 2 \) nm; buried oxide, \( t_{box} = 100 \) nm; silicon layer width, \( W_{fin} = 15 \) nm; and extensions length, \( L_{ext} = 30 \) nm.

Many simulation series were done varying the fin height \( H_{fin} \) from a large value down to nanowires, as 100, 70, 50, 30, 15 and 10 nm for several channel lengths from long to short channel, as 500, 300, 200, 100, 50 and 30 nm.

The lineal transfer characteristic was simulated for \( V_{DE} = 50 \) mV and the transfer one in saturation for \( V_{DS} = 1.5 \) V. The output characteristic was obtained for \( V_G = 1 \) V.

With the purpose of reducing the paper length we present a summary of all obtained results.

First of all, we start the analysis for transistors with several fin heights. Fig. 2 shows the behavior of the normalized simulated and modeled current for a channel of 50 nm in linear regime, at

![Fig. 2. Normalized transfer characteristic at \( V_G = 50 \) mV for several fin heights.](image)

\[ Symbols: 3D simulation \] Lines: Model
\[ L = 50 \text{ nm} \]

\[ V_{DE} = 50 \text{ mV} \]

![Fig. 3. Normalized transfer characteristic at \( V_G = 1.5 \) V for several fin heights.](image)

\[ Symbols: 3D simulation \] Lines: Model
\[ L = 50 \text{ nm} \]
\[ V_{DE} = 1.5 \text{ V} \]

![Fig. 4. Comparison of modeled and simulated normalized transconductances at \( V_G = 50 \) mV (left axis) and 1.5 V (right axis) for several fin heights.](image)

\[ Symbols: 3D simulation \] Lines: Model
\[ L = 50 \text{ nm} \]
\[ V_{DE} = 50 \text{ mV} \] and \[ V_{DE} = 1.5 \text{ V} \]
Results show that the output conductance is expected from analyzing Eq. (11), as an important role in the electrostatic control of the device. Also, comparing the simulated and modeled output characteristics (right axis) and Fig. 5.

From Fig. 4 the normalized transconductance behavior is shown for linear and saturation cases, at \( V_D = 50 \text{ mV} \) and \( 1.5 \text{ V} \), respectively. At low drain voltage, the peak of the \( g_{m} \) curve is governed mainly by the bulk mobility. The modeled results match very well with the simulated ones. In addition, the figure shows the transconductance for the saturation case. At the same time, in Fig. 5 the normalized output characteristic and its conductance are shown for \( V_C = 1 \text{ V} \). From these figures, one can observe that there is a slow decay in the saturation current for greater heights 100, 70 and 50 nm cases. Again, one can observe that nanowire devices exhibit a more marked difference respect to the other ones.

Summarizing, the current reduction in transfer characteristics for the nanowire of 10 nm of height respect to the TGJLT of \( V_D = 50 \text{ mV} \), while Fig. 7 shows it at \( V_C = 1.5 \text{ V} \). As can be seen, the simulated curves and the modeled ones match very well. Transconductance is displayed in the Fig. 8, where one can note a good agreement in linear and saturation operation. The output characteristic presented in Fig. 9 gives excellent results and also the output conductance follows very well the simulated curves. From all these plots, one can observe that the model can accurately reproduce the simulations results for several channel lengths with very small fin height, describing the short channel length in a wide range from 500 nm to 30 nm. Fig. 6 shows the current behavior at \( V_D = 50 \text{ mV} \), while Fig. 7 shows it at \( V_C = 1.5 \text{ V} \). As can be seen, the simulated curves and the modeled ones match very well. Transconductance is displayed in the

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<th>( H_{\text{Fin}} ) (nm)</th>
<th>( \mu_0 ) ((\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}))</th>
<th>( R ) ((\Omega))</th>
<th>( n )</th>
<th>( \beta_{1} ) ((\text{V}^{-1}))</th>
<th>( \beta_{2} ) ((\text{V}^{-1}))</th>
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Fig. 5. Comparison of simulated and modeled output characteristics (right axis) and output conductance (left axis) at \( V_C = 1 \text{ V} \) for several fin heights.

Fig. 6. Simulated and modeled transfer characteristics in linear and semilog scale at \( V_D = 50 \text{ mV} \) for several channel lengths.

Fig. 7. Simulated and modeled transfer characteristics in linear and semilog scale at \( V_C = 1.5 \text{ V} \) for several channel lengths.
channel effects as $V_T$ roll-off, subthreshold slope and DIBL as well as the velocity saturation effect and the mobility degradation.

Finally, in general aspects Fig. 10 presents the results obtained for the threshold voltage for long transistors modeled by (11), which considers the change of the fin height, where it can be seen that the model predicts very well the behavior trend. On the other hand, the threshold voltage roll-off is also well reproduced. It was observed that there is a very small change in $S$ as $H_{fin}$ is reduced while the DIBL varies within 10 mV/V. The extraction of $V_T$ was done by the second derivative method. As can be seen, the proposed model can predicts the changes of $V_T$ from DG to nanowire transistors for long and short channel devices.

8.2. Experimental results and discussion

The proposed compact drain current model was also validated with measurements of experimental devices fabricated at CE-LETI on SOI wafers with (100) orientation with 145 nm of buried oxide following the process described in [28] and reported in [11]. The one single fin devices are fabricated with PolySi/TiN as gate metal stack and 1.2 nm EOT HfSiON as gate dielectric material. The effective dimensions for the geometrical parameters $H_{fin}$ and $W_{fin}$ are 10 and 20 nm, respectively. Doping concentrations of $5 \times 10^{18}$ and $1 \times 10^{19}$ cm$^{-3}$ have been implanted in the single fin devices with channel length dimensions of 30, 40, 50, 70 and 90 nm.

On the simulation case, one can work with Boltzmann statistics in order to make easier the analysis and time computing. Real devices, with heavy doping concentrations as the JLT case, present incomplete impurity ionization. In silicon as semiconductor with doping concentration above $3.6 \times 10^{18}$ cm$^{-3}$, Boltzmann statistics overestimates the carrier concentration. For this reason, the Pseudo-Boltzmann model [29] was used to calculate the carrier concentration. This method allows obtaining carrier concentrations as when Fermi Dirac statistics is used, but using the following expressions:

$$n_m = \begin{cases} \frac{N_e e^{c/kT}}{C_0} & \text{for } \gamma_C < -2.03 \\ a \cdot N_e e^{c/kT} & \text{for } \gamma_C \geq -2.03 \end{cases}$$

(35)

where $\gamma_C = \frac{E_F - E_C}{kT}$.

In this case the values used for parameters $a$ and $b$ were: $a = 0.765$ and $b = 0.8684$.

Since the above expressions have the same mathematical structure as Boltzmann one, they can be used for calculating the currents, without modifying the mathematical expressions of the model.

Fig. 11 shows the normalized $I$–$V$ characteristics at $V_D = 50$ mV at linear and semilog scale, where the sub-$V_T$ behavior, the subthreshold slope degradation and the fall of the threshold voltage
On the other hand, a fairly well modeling for saturation at shift influence of the interface charges on the flat band voltage. are seen, due to the channel length scaling along with the small shift influence of the interface charges on the flat band voltage. The output characteristic for current and conductance were also impacted of the high interface charge. Derivatives of the current at linear and saturation are very well described showing the results in Fig. 13 and in the insert one, respectively. The maximum mobility drops very drastically in the transconductance at 50 mV, as a result of the impact of the parallel electric field on the carrier acceleration. The output characteristic for current and conductance were also modeled, see Fig. 14. Even though the current decreases with scaling, the $I-V$ plot makes possible to observe with much detail the powerful impact of the high series resistance on the device performance.

In Fig. 15 are displayed the DIBL and subthreshold slope degradation for the two types of measured transistors with different doping concentration. The results show a better agreement for a lower $N_{D}$, however, the tendency is very good reproduced. DIBL and $S$ were extracted as in [13]. From all the results presented, the proposed model is able to describe suitably the static behavior of TGJLT as well as nanowires, with only 8 parameters.

**9. Conclusion**

A new charge-based compact analytical model for triple gate JLT is presented, that includes the short channel effects and can be also used for double gate JLT. This model uses only 8 adjusting parameters and is included the influence of the fin height on the semiconductor capacitance. The main short channel effects: threshold voltage roll-off, subthreshold slope variation, DIBL and channel length modulation are also included, as well as, the mobility degradation, velocity saturation and series resistance. An expression for the threshold voltage expression is also presented. The model is supported by 3-D simulations and experimental measurements. Simulations results were validated for devices corresponding to DG case with 100 nm of height down to nanowire transistors with 10 nm height. Measured nanowire transistors had doping concentrations of $5 \times 10^{18}$ and $1 \times 10^{19}$ cm$^{-3}$. The channel length was scaled from long channel to short channel dimensions in both the simulations and fabricated devices. The validations confirm that the model is appropriate for JLT DC circuits’ analysis.

**Acknowledgements**

This work was supported at CINVESTAV in Mexico by CONACYT Project 236887. Marcelo A. Pavanello and Bruna C. Paz
acknowledge FAPESP and CNPq for the financial support. The authors acknowledge to the General Coordination of Information and Communications Technologies (CGSTIC) at CINVESTAV for providing HPC resources on the Hybrid Cluster Supercomputer “Xiuhcoatl”, that have contributed to the research results reported in this paper. The experimental junctionless devices were fabricated by CEA-LETI in the framework of the European project SQWIRE under Grant Agreement N° 257111, finished in September 2013. The authors are grateful to the staff of CEA-LETI for the fabrication and to Prof. Jean-Pierre Colinge and Dr. Isabelle Ferain for supplying of junctionless nanowire transistors.

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