

Verilog-A implementation of a double-gate junctionless compact model for DC circuit simulations

This content has been downloaded from IOPscience. Please scroll down to see the full text.

2016 Semicond. Sci. Technol. 31 075002

(<http://iopscience.iop.org/0268-1242/31/7/075002>)

View [the table of contents for this issue](#), or go to the [journal homepage](#) for more

Download details:

IP Address: 148.247.101.66

This content was downloaded on 23/11/2016 at 21:02

Please note that [terms and conditions apply](#).

You may also be interested in:

[Double-gate junctionless transistor model including short-channel effects](#)

B C Paz, F Ávila-Herrera, A Cerdeira et al.

[Automatic parameter extraction techniques in IC-CAP for a compact double gate MOSFET model](#)

Ghader Darbandy, Thomas Gneiting, Heidrun Alius et al.

[Short channel effects in graphene-based field effect transistors targeting radio-frequency applications](#)

Pedro C Feijoo, David Jiménez and Xavier Cartoixà

[Extrinsic resistances in modelling of MODFETs](#)

B González, A Hernández, J García et al.

[Compact drain-current model for reproducing advanced transport models in nanoscale DG MOSFETs](#)

M Cheralathan, C Sampedro, J B Roldán et al.

[A carrier-based analytic drain current model incorporating velocity saturation for undoped SRG MOSFETs](#)

Lining Zhang, Yan Guan, Wang Zhou et al.

Verilog-A implementation of a double-gate junctionless compact model for DC circuit simulations

J Alvarado^{1,4}, P Flores², S Romero², F Ávila-Herrera³, V González²,
B Soto-Cruz¹ and A Cerdeira³

¹ Research Center of Semiconductor Devices, Science Institute, Benemérita Universidad Autónoma de Puebla, Av. San Claudio, Col. San Manuel, Puebla 72570, México

² Electronic Science Faculty, Benemérita Universidad Autónoma de Puebla, Av. San Claudio, Col. San Manuel, Puebla 72570, México

³ Solid State Electronics section, CINVESTAV, Av. Politecnico, Mexico City, México

E-mail: joaquin.alvarado@correo.buap.mx

Received 5 March 2016

Accepted for publication 20 April 2016

Published 31 May 2016



CrossMark

Abstract

A physically based model of the double-gate junctionless transistor which is capable of describing accumulation and depletion regions is implemented in Verilog-A in order to perform DC circuit simulations. Analytical description of the difference of potentials between the center and the surface of the silicon layer allows the determination of the mobile charges. Furthermore, mobility degradation, series resistance, as well as threshold voltage roll-off, drain saturation voltage, channel shortening and velocity saturation are also considered. In order to provide this model to all of the community, the implementation of this model is performed in Ngspice, which is a free circuit simulation with an ADMS interface to integrate Verilog-A models. Validation of the model implementation is done through 2D numerical simulations of transistors with 1 μm and 40 nm silicon channel length and 1×10^{19} or $5 \times 10^{18} \text{ cm}^{-3}$ doping concentration of the silicon layer with 10 and 15 nm silicon thickness. Good agreement between the numerical simulated behavior and model implementation is obtained, where only eight model parameters are used.

Keywords: junctionless transistors, compact modeling, Verilog-A, circuit simulation

(Some figures may appear in colour only in the online journal)

1. Introduction

Due to the uniformly doped nanowire without junctions, as well as a wrap-around gate, junctionless transistors (JLT) are one of the most promising candidates to cover the ITRS projections for 20 nm downscaling [1]. JLT transistors can be fabricated in a similar way to FinFETs transistors [1]. However, their behaviour can be basically related to a resistor in which the mobile carrier density can be modulated by the gate. As a result, a trade-off between a heavily doped and a thin silicon layer has to be made in order to increase the device conductivity, as well as to ensure a full depletion and

current cut-off. Furthermore, similar to FinFETs, JLTs can work as Double Gate or Tri-Gate MOSFETs [2–6].

In order to simplify the analysis of its current-voltage behavior, a double-gate JLT (DJLT) has to be considered such as in [7–10], where numerical-analytical or complete analytical models are presented. Most models have been developed at different regions of operation [11–13] and a few for all regions [14–17]. It is worth pointing out that one of the main problems in the modeling of the DJLT is the transition from the depletion mode to accumulation mode, because of its different physical behaviors. The JLT is fully depleted below threshold voltage and the device is turned-off, as the gate voltage is increased, the electron concentration also increases until it reaches the threshold. If the gate voltage is increased further, the entire

⁴ Author to whom any correspondence should be addressed.

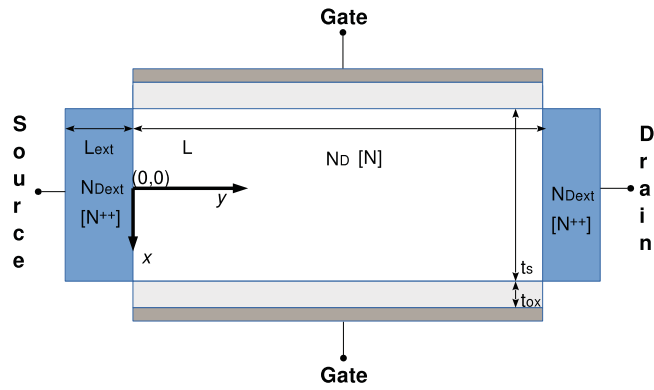


Figure 1. Double-gate junctionless structure.

cross-section of the transistor channel becomes neutral. As a result, the device is no longer depleted and the flat-band voltage is reached. In fully depleted as well as at partially depleted conditions, the current is defined by the charge transport at or near the center of the silicon layer (body current) [18]. However, for gate voltages larger than the flat-band condition, the accumulation mode is reached and an additional current starts to flow underneath the insulator while the body current remains.

Recently we presented a drain current model for DJLT considering the total mobile charge in the channel from the center to the surface [19]. Afterwards, short-channel effects were included such as the increase of the body potentials due to the drain bias, mobility degradation, carrier velocity saturations and series resistance. In this paper we present the implementation of this analytical DJLT model in Verilog-A, which allows its introduction in commercial circuit simulators for circuit design. The implementation in Verilog-A is also validated using simulations in ATLAS [20].

2. Model description

2.1. Potentials

The 2D structure of the DJLT under analysis is shown in figure 1, where L is the gate length, W is the gate width, t_{ox} is the equivalent oxide thickness (EOT), t_s is the silicon thickness of the transistor and L_{ext} is the silicon extension at source and drain, which have a higher doping concentration N_{Dext} comparing with the one below the gate N_D . According to this 2D structure, the difference of the potentials of the silicon layer between the surface, ψ_s , and the center, ψ_o , normalized with respect to the thermal voltage, ψ_t , can be calculated as shown in (1) according to [21].

$$\alpha = \alpha_{bt} + LW \left[-\alpha_{bt} \cdot e^{-\alpha_{bt}} \cdot e^{\frac{\psi_s - V}{\psi_t}} \right] \quad (1)$$

where α_{bt} is the normalized difference of potentials in deep subthreshold, V is the channel voltage and LW is the Lambert function. Furthermore, when a gate voltage, V_G , and drain voltage, V_D , are applied, they will affect the surface potential as:

$$V_G - V_{FB} = \psi_s + \text{sign}(\alpha) \cdot \psi_t \cdot \beta \cdot \sqrt{e^{\frac{\psi_s - V_D}{\psi_t}} - \xi \cdot \alpha - 1} \quad (2)$$

where $\beta = \sqrt{\frac{q_b}{2\gamma}}$, $\xi = \left(1 - \frac{1}{\alpha_{bt}}\right)$, $q_b = \frac{qN_D t_s}{C_{ox} \psi_t}$ is the normalized fixed charge in the silicon layer, C_{ox} is the gate capacitance per unit area, C_s is the silicon capacitance per unit area and $\gamma = \frac{C_{ox}}{4C_s}$.

Since it is not possible to get an analytic solution for the surface potential in (2), an iterative solution is showed in [18], where a precision better than 0.01% is obtained with a maximum of two iterations.

Moreover, the normalized difference of potentials at the threshold voltage is equal to:

$$\alpha_T = \frac{\alpha_{bt}}{1 - \alpha_{bt}} \left[1 - \alpha_{bt} \left(1 - \frac{1}{2q_b} \right)^2 \right] \quad (3)$$

2.2. Mobile charges

Considering just one half of the channel, an analytical expression of the mobile charge from the center to the surface of the silicon layer as a function of the potentials is found through solving Poisson's equation:

$$q_n = -\text{sign}(\alpha) \cdot \beta \cdot \sqrt{e^{\frac{\psi_s - V}{\psi_t}} - \xi \cdot \alpha - 1} - \frac{q_b}{2} \quad (4)$$

Since DJLT presents two regimes of operation: depletion and accumulation, the drain current, I_D , has been obtained by decoupling (4) at these conditions, in order to ease the integration. Then, at the depletion region, the total charge is a function of α , as follows:

$$q_{dep} = \beta \cdot \sqrt{e^{\xi \alpha} - \xi \cdot \alpha - 1} \quad (5)$$

Whereas in accumulation region, the total charge is a function of ψ_s , which is given as:

$$q_{acc} = -\beta \cdot \sqrt{e^{\frac{\psi_s - V}{\psi_t}} - \frac{\psi_s - V}{\psi_t} - 1} \quad (6)$$

Finally, a continuous mobile charge expression from depletion to accumulation is obtained using the tanh function as follows:

$$q_{tot} = \frac{1}{2} q_{dep} \{ 1 - \tanh[25(V_G - (V_{FB} + V_D))] \} + \frac{1}{2} q_{acc} \{ 1 + \tanh[25(V_G - (V_{FB} + V_D))] \} \quad (7)$$

2.3. Drain current

As already mentioned, I_D is obtained by integrating all of the electron mobile charge inside the silicon layer (4) by:

$$I_D = 2 \cdot \frac{W}{L} \cdot C_{ox} \cdot \mu \cdot \int_{V_s}^{V_D} q_n \cdot dV \quad (8)$$

Since (4) cannot be integrated in simple mathematical steps, the mobile charges for accumulation and depletion regimes were used. Final expressions of the drain current according to [18] in below threshold, I_{dep_bt} , as well as in above threshold,

$I_{\text{dep_at}}$, are equal to:

$$I_{\text{depbt}} = -0.03 \cdot K \cdot \psi_t \cdot \left\{ \frac{1}{2} (q_{\text{totS}}^2 - q_{\text{totD}}^2) + \frac{\beta}{\xi} [SaN(\xi\alpha_S) - SaN(\xi\alpha_D)] \right\} \quad (9)$$

$$I_{\text{depat}} = K \left\{ \frac{q_b}{2} [V_D - V_S + 0.01(1.1 \cdot 10^{-4} - V_D)] + \frac{\psi_t}{2} (q_{\text{totS}}^2 - q_{\text{totD}}^2) + \frac{\psi_t \beta}{\xi} [SaN(\xi\alpha_S) - SaN(\xi\alpha_D)] - \psi_t \beta [Sb(V_S) - Sb(V_D)] \right\} \quad (10)$$

$$\mu_S = \frac{\mu_0}{1 + [\theta_1(V_G - V_{FB}) + \theta_2 V_{\text{Deff}}] \cdot \frac{1}{2} \{1 + \tanh[5(V_G - V_{FB})]\}} \quad (15)$$

where $q_{\text{totS,D}} = q_{\text{tot}}(V_G, V_{S,D})$, $\alpha_{S,D} = \alpha(V_G, V_{S,D})$ and $K = 2 \frac{W}{L} C_{\text{ox}} \mu$. As a result, a continuous expression for the drain current in the depletion regime is given by:

$$I_{\text{dep}} = \frac{1}{2} I_{\text{dep_bt}} \{1 - \tanh[30(V_G - V_T)]\} + \frac{1}{2} I_{\text{dep_at}} \{1 + \tanh[30(V_G - V_T)]\} \quad (11)$$

Whereas, the current in the accumulation regime is calculated as:

$$I_{\text{acc}} = K \left\{ \frac{q_b}{2} (V_D - V_S) + \frac{\psi_t}{2} (q_{\text{totS}}^2 - q_{\text{totD}}^2) + \psi_t \beta \left[SaP \left(\frac{V_G - V_{FB} - V_S}{\psi_t} + q_{\text{totS}} \right) \right] - \psi_t \beta \left[SaP \left(\frac{V_G - V_{FB} - V_D}{\psi_t} + q_{\text{totD}} \right) \right] \right\} \quad (12)$$

Also, expressions for functions SaN , Sb , SaP are defined in [18]. The final expression for the total drain current valid in both regimes is equal to:

$$I_{\text{tot}} = \frac{1}{2} I_{\text{dep}} \{1 - \tanh[100(V_G - (V_{FB} + V_D))]\} + \frac{1}{2} I_{\text{acc}} \{1 + \tanh[100(V_G - (V_{FB} + V_D))]\} \quad (13)$$

2.4. Short channel effects

The expression for the current (13) is used as the core model for DJLT. With the channel length reduction, 2D effects appear near the source and drain producing the so-called Short Channel Effects (SCE). In our core model, the effects of velocity saturation, channel length modulation, Drain Induced Barrier Lowering (DIBL) and subthreshold degradation were included, describing the process in the following sections:

2.4.1. Velocity saturation and variable mobility. For short channel devices the carrier velocity saturation v_{sat} obtained at the critical electrical field along the channel, gives a surface mobility reduction as:

$$\mu_{\text{eff}} = \frac{\mu_S}{\sqrt{1 + \left(\frac{\mu_S \cdot V_{\text{Deff}}}{L \cdot v_{\text{sat}}} \right)^2}} \quad (14)$$

where the effective mobility is given by the superposition of two parallel currents: one flowing through the center with a constant mobility μ_0 and the other at the surface of the silicon layer, which presents scattering effects. As a result, surface mobility can be calculated as in [18]:

where θ_1 and θ_2 are adjusting parameters defining the mobility degradation for $V_G > V_{FB}$. Furthermore, the effective drain voltage V_{Deff} as well as the drain saturation voltage V_{Dsat} are defined by:

$$V_{\text{Deff}} = V_{\text{Dsat}} + \frac{1}{2} [V_D - V_{\text{Dsat}} + \psi_t - \sqrt{(V_D - V_{\text{Dsat}} + \psi_t)^2 + 4\psi_t V_{\text{Dsat}}}] \quad (16)$$

$$V_{\text{Dsat}} = \begin{cases} V_G - V_{T0} & \text{for } L \geq 300 \text{ nm} \\ 0.08 + \eta (L v_{\text{sat}})^{0.33} (V_G - V_{T0}) & \text{for } L < 300 \text{ nm} \end{cases} \quad (17)$$

where η is an adjusting parameter. The threshold voltage for long channel transistors is given by:

$$V_{T0} = V_{FB} - \psi_t \left[\frac{q_b}{2} - \frac{1}{4} - \alpha_T - \ln \left(1 - \frac{\alpha_T}{\alpha_{bt}} \right) \right] \quad (18)$$

2.4.2. Subthreshold characteristics. In subthreshold regime the channel electrostatic potential of the DJLT is obtained by considering that the total charge is approximately equal to the fix charge (full depletion). In order to consider this regime, the subthreshold slope degradation as well as the SCE in the threshold voltage, such as the roll-off and the DIBL, an effective gate voltage, V_{Geff} , has to be introduced instead of V_G , and is expressed as:

$$V_{\text{Geff}} = V_G + \psi_{0\text{min}} - \psi_{0p} \quad (19)$$

where the minimum value of the potential, $\psi_{0\text{min}}$, is defined according to [18] by:

$$\psi_{0\text{min}} = \psi_{0p} + \frac{\sqrt{2U_S U_{\text{Dc}} \cosh\left(\frac{L}{t_n}\right) - U_S^2 - U_{\text{D}}^2}}{\sinh(L/t_n)} \quad (20)$$

Table 1. Model parameters and extracted values for model simulations.

L	Parameters									
	$N_D \cdot 10^{19}$ (cm^{-3})	t_s (nm)	μ_0 (cm^2/Vs)	θ_1 (V^{-1})	θ_2 (V^{-1})	R (Ω)	n	λ	η	$v_{\text{sat}} \cdot 10^7$ (cm^{-1})
1 μm	1	10	100	-0.02	0.02	216	0.3	0	0.15	1
1 μm	0.5	10	145	-0.22	0.23	530	0.85	0.75	0.142	0.75
1 μm	0.5	15	140	-0.02	0.05	167	0.7	0	0.118	1
40 nm	1	10	98	0.02	0.32	45	0.86	0.35	0.153	1.23
40 nm	0.5	10	140	-0.23	0.93	60	0.9	0.24	0.136	1.4
40 nm	0.5	15	140	0	0.05	33	0.4	0.28	0.112	1.2

where the subthreshold potential at the center of the silicon layer for a long channel device $\psi_{0p} = V_G - V_{\text{FB}} + t_n^2 \frac{qN_D}{\epsilon_s}$, t_n is the double gate natural length [5], $U_S = V_{\text{biefS}} - \psi_{0p}$, $U_D = V_{\text{biefD}} - \psi_{0p}$. The built-in effective voltage, considering the effect of source and drain extensions according to [14], is given by:

$$V_{\text{bief},S/D} = \psi_{0p} - t_n^2 \frac{qN_{\text{Dext}}}{\epsilon_s} \times \left(1 - \sqrt{1 + \frac{2\epsilon_s(V_{\text{biS0}} + V_{S/D} - \psi_{0p})}{qN_{\text{Dext}}t_n^2}} \right) \quad (21)$$

where $V_{\text{biS0}} = V_A + \psi_f$ is the built-in voltage at the source/channel interface, ψ_f is the Fermi level in the channel and V_A is the constant parameter. Finally, threshold voltage roll-off is given through a threshold voltage correction of V_T as:

$$\Delta V_T = \frac{V_{\text{biS0}} - \left(V_{T0} - V_{\text{FB}} + t_n^2 \frac{qN_D}{\epsilon_s} \right)}{\cosh(L/2t_n)} \quad (22)$$

2.4.3. Channel length modulation. Another effect produced by the increment in the electrical field along the channel is the channel length modulation (CLM), which is consider as:

$$\Delta L = \lambda \sqrt{\frac{2\epsilon_s}{qN_D} (V_D - V_{\text{Def}})} \quad (23)$$

2.4.4. Series resistance. The series resistance effect due to the source and drain extensions has been introduced into the current factor K of (12) as:

$$KK = \frac{1}{1 - \Delta L/L} \cdot \frac{\psi_T K}{1 + KR(V_{\text{Geff}} - V_T - nV_{\text{Def}})} \cdot \frac{1}{2} \cdot \{1 + \tanh[2(V_G - V_T - nV_{\text{Def}})]\} \quad (24)$$

where R is the sum of the source and drain resistances and n is the adjusting parameter. The drain current is calculated using the effective gate voltage, the effective drain voltage and KK instead of K in expressions (9–12).

3. Verilog-A implementation of the DJLT model in circuit simulators

In order to assess the validity of the DJLT model to perform DC circuit simulations, we have implemented the aforementioned equations in Verilog-A language (see appendix A). Thanks to its support for different modules where each one can be described mathematically in terms of its terminals and external parameters applied to the module, Verilog-A language seems to be the best tool for describing compact modeling. The descriptive code of the model was introduced in Ngspice according to [22]. It is worth pointing out that Ngspice is a free circuit simulator to integrate Verilog-A code. However, due to its limited built-in functions and external tools to perform the compilation such as the ADMS interface, a more complex implementation has to be done in order to obtain similar results as in commercial tools, as well as to avoid convergence problems. Validation of the implementation of the DJLT model in Verilog-A was performed through 2D numerical simulations in order to obtain similar results as in [18].

As good practice, it is necessary to define the built-in functions which will be used several times along the code. Those are located at the beginning of the code (lines 9–229). It is worth pointing out that the way the functions are defined can allow the user to compile them either in open source software, such as Ngspice, or in commercial software without making any change. Therefore, the model parameters are listed in lines 240–260 and also shown in table 1.

Furthermore, the difference of the potentials at the threshold voltage (3) is first determined in order to calculate the threshold voltage (lines 371–380). Afterwards, subthreshold behavior is calculated by the effective gate voltage (18) in lines

382 to 394, in which the main SCE are covered. The effective drain voltage is determined due to the saturation velocity (lines 395–414). Once the effective voltages at the drain and gate as well as the threshold voltage are known, it is possible to

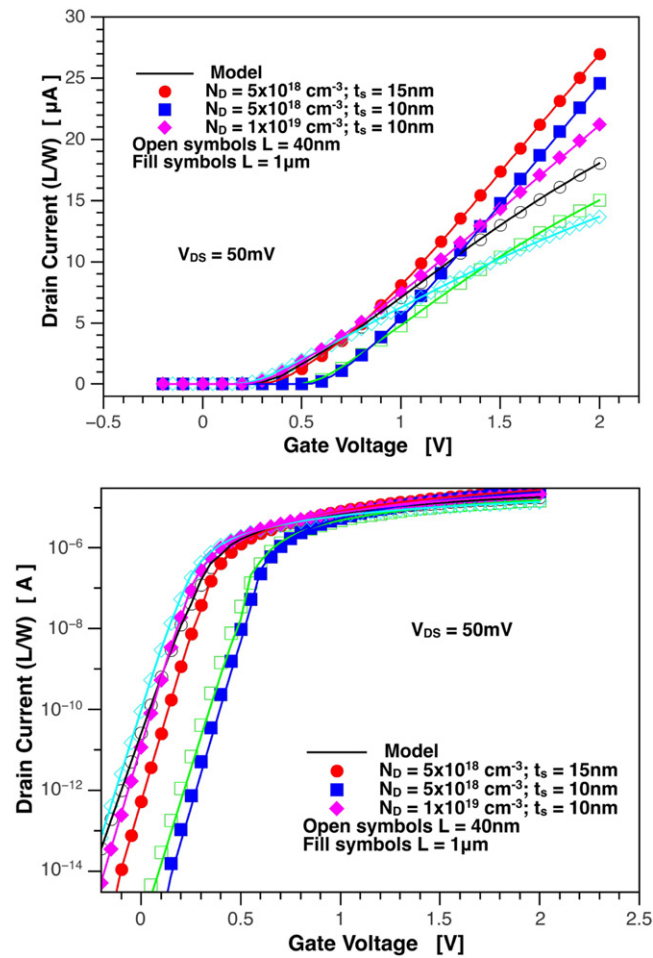


Figure 2. Comparison of simulated (symbols) and model implemented (lines) transfer characteristics at $V_D = 50 \text{ mV}$ in linear (top) and in subthreshold (bottom). Open symbols correspond to 40 nm channel length, and filled symbols to $1 \mu\text{m}$.

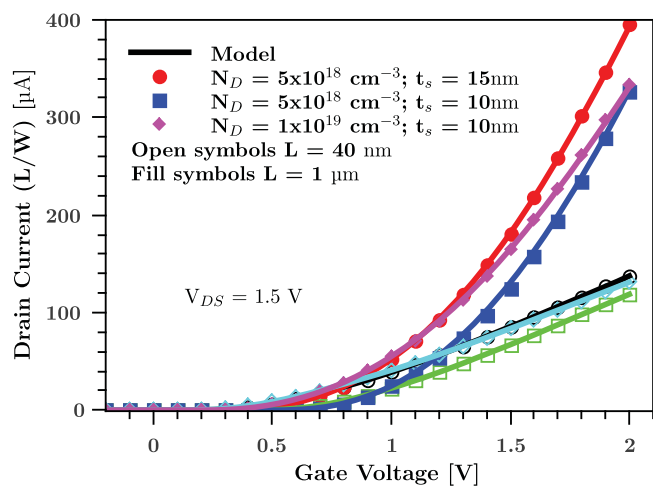


Figure 3. Comparison of simulated (symbols) and model implemented (lines) transfer characteristics at $V_D = 1.5 \text{ V}$. Open symbols correspond to 40 nm channel length, and filled symbols to $1 \mu\text{m}$.

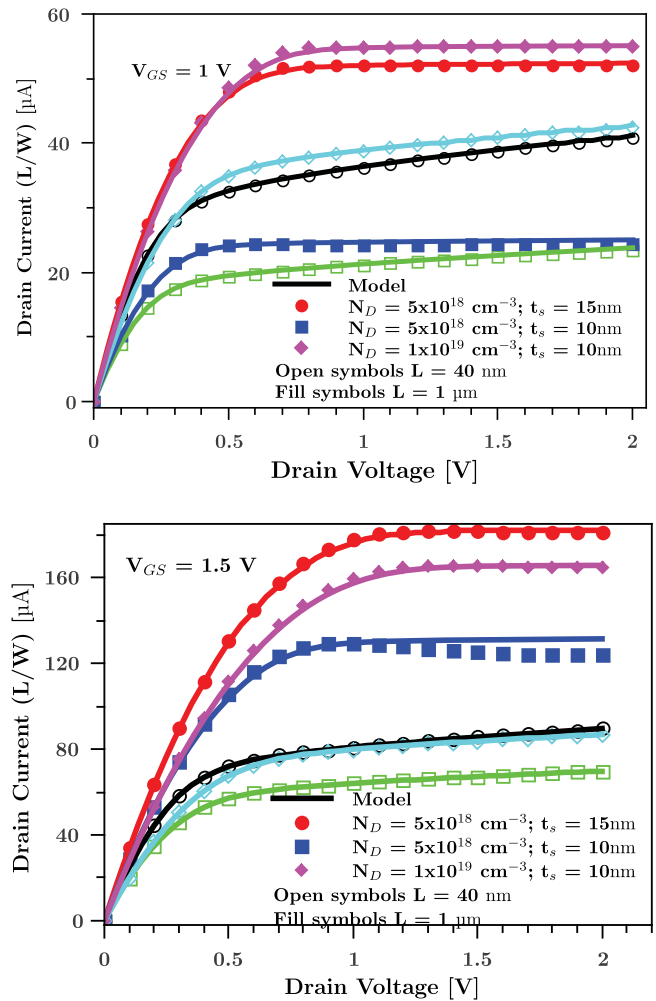


Figure 4. Comparison of simulated (symbols) and model implemented (lines) output characteristics at. Open symbols correspond to 40 nm channel length, and filled symbols to $1 \mu\text{m}$.

calculate the potentials at the center of the silicon layer and at the surface close to the drain and to the source (lines 415–433).

Then, potentials are used to determine the mobile charges in the depletion regime and in accumulation (lines 434–466). Finally, the drain current is calculated (lines 480–506), through considering the effective mobility (lines 467–470), CLM (lines 471–474) and series resistance (lines 475–479).

4. Results and discussion

The implemented description for DJLT in Verilog-A was introduced in the circuit simulator Ngspice. The results obtained from the simulations were compared with ATLAS simulations. Double-gate Junctionless transistors with two different gate lengths ($L = 1 \mu\text{m}$ and 40 nm) with 10 nm or 15 nm of silicon layer thickness and $5 \times 10^{18} \text{ cm}^{-3}$ or $1 \times 10^{19} \text{ cm}^{-3}$ doping

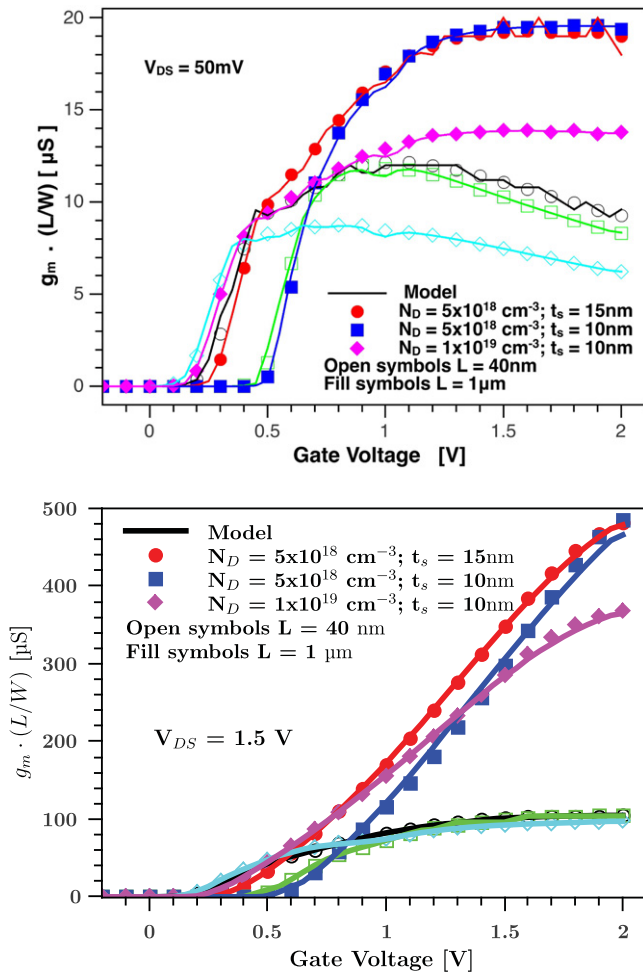


Figure 5. Comparison of simulated (symbols) and model implemented (lines) transconductance characteristics at $V_D = 50$ mV (top) and at $V_D = 1.5$ V (bottom). Open symbols correspond to 40 nm channel length, and filled symbols to $1 \mu\text{m}$.

concentration were considered. Also, all simulated transistors have 2 nm gate oxide thickness and $1 \mu\text{m}$ gate width as well as 5.2 eV work function. Table 1 shows the extracted parameters of the transistors used in Ngspice simulations.

Figure 2 (top) shows the comparison of simulated and modeled transistors in linear normalized transfer characteristic at $V_{DS} = 50$ mV. Furthermore, figure 2 (bottom) shows the semilogarithmic characteristic in order to observe the subthreshold region. Good agreement from depletion to accumulation is obtained. Also, good agreement between the modeled and simulated transistors is obtained in figure 3 for normalized transfer characteristics at $V_{DS} = 1.5$ V.

Normalized output characteristics are shown in figure 4 for two different gate voltages, whereas normalized transconductance at $V_{DS} = 50$ mV and 1.5 V are shown in figure 5. Finally, normalized conductance at $V_{GS} = 1$ V is shown in figure 6.

As can be seen from linear to saturation conditions, continuous modeled characteristics show good agreement with the simulated data.

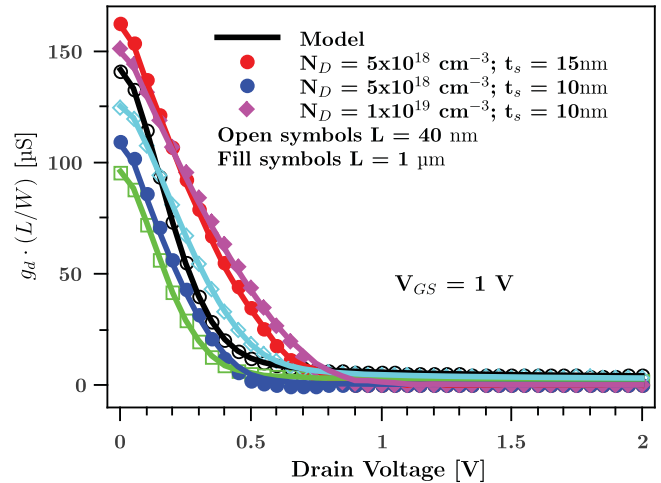


Figure 6. Comparison of simulated (symbols) and model implemented (lines) conductance characteristic at $V_G = 1$ V. Open symbols corresponds to 40 nm channel length, and filled symbols to $1 \mu\text{m}$.

Conclusion

In this work, we present the implementation of the DJLT model in Verilog-A, which considers short channel effects, variable mobility and series resistance. Development and implementation of special subfunctions in Verilog-A were necessary to be performed, such as Lambert and Gauss’s hypergeometric functions, in order to obtain good agreement between analytical expressions and modeled simulations, as well as to obtain fast convergence. The expression for the calculation of the variable mobility, as well as short channel effects that include channel length modulation, DIBL, V_1 roll-off, subthreshold variation as well as carrier velocity saturation and series resistance were also implemented. Modeled and simulated transfer characteristics in linear and saturation regions, as well as the output characteristics, show good agreement in all operating regions, which allows us to confirm that the Verilog-A implemented compact analytical model for DJLT presented in this work is able to describe digital and mixed electronic circuits operating in DC.

Acknowledgments

This work was supported at BUAP by VIEP project No. 275, as well as at CINVESTAV by CONACYT project 236887.

Appendix A

```

1 //JUNCTIONLESS TRANSISTOR
2 //*****//
3 //***** Functions Definition *****//
4 //*****//
5 /** Libraries **/
6 'include "discipline.h"

```

(Continued.)

```

7 'include "constants.h"
8 /** Constant **/
9 'define q (1.60219E-19)
10 'define Eo (8.85419E-14)
11 'define ko (3.9)
12 'define kB (1.38066E-23)
13 'define ks (11.8)
14 'define T (300)
15 /** Square Root Function **/
16 'define ffsqrt (x1, fsqrt1)\
17 if (x1>0)\
18     fsqrt1=sqrt (x1);\
19 else\
20     fsqrt1=0;
21 /** Sign Function **/
22 'define fsgn (datain,sgn)\
23 if (datain==0)\
24     sgn=0;\
25 else\
26     sgn=datain/abs(datain);
27 /** Lambert Funtion **/
28 'define flambert(z,w)\
29 if(z==0)\
30     fl1=1;\
31 else\
32     fl1=0;\
33 tmp1=ln(fl1+z);\
34 'ffsqrt(2*(exp(1)*z+1),flamx1);\
35 if(tmp1>0)\
36     w=tmp1 - ln(tmp1);\
37 else\
38     w=flamx1 - 1;\
39     kl=1;\
40     while (kl<=26) begin \
41         c11=exp(w);\
42         c21=w* c11 - z;\
43         if(w!= 1) begin\
44             f121=1;\
45         end else begin\
46             f121=0;\
47         end\
48         w11=w + f121;\
49         dw1=c21/(c11* w11 - 0.5 * ((w + 2 ) *
50             (c21 / w11) ) );\
51         w=w - dw1;\
52         kl=kl+1;\
53     end
54 /** Surface Potential calculation through 3th order
55     Newton-Raphson **/
56 'define fht(htVg,htVfb,htx,htB,htalphasu,htBeta,htepsilon,htVd,
57     htphit,rht)\
58 fhtx1 = htB* exp(htx);\
59 'flambert(fhtx1,fhtx2);\
60 alpha1=htalphasu+fhtx2;\
61 'fsgn(alpha1,fhtx3);\
62 'ffsqrt(exp(htx)-(alpha1*hte epsilon)-1,fhtx4);\
63 ft=htx+((fhtx3*htBeta)*fhtx4)-((htVg-(htVfb+htVd))/
64     htphit);\
65 'flambert(htB*exp(htx),fhtx5);\
66 'flambert(htB*exp(htx),fhtx6);\
67 alpha1=fhtx5/(1+fhtx6);\

```

(Continued.)

```

64 'fsgn(alpha1,fhtx7);\
65 'ffsqrt(exp(htx)-alpha1*hte epsilon-1,fhtx8);\
66 ft1=1+((htBeta*fhtx7)/2)*((exp(htx)-hte epsilon*alpha1)/
67     (fhtx8));\
68 'flambert(htB*exp(htx),fhtx9);\
69 'flambert(htB*exp(htx),fhtx10);\
70 alpha2=fhtx9/pow(1+fhtx10,3);\
71 'fsgn(alpha1,fhtx11);\
72 'ffsqrt(exp(htx)-alpha1*hte epsilon-1,fhtx12);\
73 ft2=-((htBeta*fhtx11)/(2))*(-(exp(htx)-hte epsilon*alpha2)/
74     (fhtx12))+((pow(exp(htx)-hte epsilon*alpha1,2)/(pow(exp(htx)
75     -hte epsilon*alpha1-1,1.5)))));\
76 'flambert(htB*exp(htx),fhtx13);\
77 'flambert(htB*exp(htx),fhtx14);\
78 'flambert(htB*exp(htx),fhtx15);\
79 alpha3=((fhtx13)*(1-2*fhtx14))/pow(1+fhtx15,5);\
80 'fsgn(alpha1,fhtx16);\
81 'ffsqrt(exp(htx)- alpha1*hte epsilon-1,fhtx17);\
82 ft3=-((htBeta*fhtx16/2)*(-(exp(htx)-hte epsilon*alpha3)/
83     fhtx17)+3/2*((exp(htx)-hte epsilon*alpha1)*((exp(htx)
84     -hte epsilon*alpha2))/pow(exp(htx)-hte epsilon*alpha
85     -1,1.5))-3/4*(pow(exp(htx)-hte epsilon*alpha1,3)/pow(exp
86     (htx)-hte epsilon*alpha1-1,2.5)));\
87 rht=-((ft/ft1)*(1+((ft*ft2)/(2*pow(ft1,2)))+(pow(ft,2))/
88     (6*pow(ft1,4)))*(3*pow(ft2,2)-ft1*ft3));
89 /** XTC Init **/
90 'define fxtc(xtcVg,xtcVd,xtcVfb,xtcVt,xtcalphasu,xtcB,
91     xtcBeta,xtcepsilon,xtcphit,xtcq,xtcNd,xtcEs,xtclambdao,
92     xtc)\
93 xtcfiop=xtcVg-xtcVfb+(xtcq*xtcNd)/(xtcEs)*pow(xtclambd-
94     dao,2);\
95 xtcalphaapprox=xtcalphasu*(1-exp((xtcfiop-xtcVd)/
96     xtcphit));\
97 xtcpsaprox=xtcalphaapprox*xtcphit+xtcfiop;\
98 xtcVx1=(xtcVg-xtcVfb-xtcVd)/xtcphit;\
99 xtcVx2=((xtcVg-(xtcVfb+xtcVd))/xtcphit)+(xtcBeta*0.8);\
100 xtcxsub1=(xtcpsaprox-xtcVd)/xtcphit;\
101 'ffsqrt(abs(1-(4/(pow(xtcBeta,2)))*(xtcVx1+1)),fxtcx1);\
102 xtcxsub2=(pow(10,-2))+xtcVx1+(((pow(xtcBeta,2))*0.5)*(-1
103     +fxtcx1));\
104 lamb1=xtcBeta/2*1.09*exp(xtcVx2/2);\
105 'flambert(lamb1,fxtcx2);\
106 xtcxar=xtcVx2-2*fxtcx2;\
107 xtcxT=(xtcxsub2*(0.5*(1-tanh((xtcVg-(xtcVfb+xtcVd))
108     *50))))+(xtcxar*(0.5*(1+tanh((xtcVg-(xtcVfb+xtcVd))
109     *50))))+0.7;\
110 xtcxF=(xtcxsub1*(0.5*(1-tanh((xtcVg-xtcVt)*50))))+(xtcxT*
111     (0.5*(1+tanh((xtcVg-xtcVt)*50))));\
112 xtcx=xtcxF;\
113 xtcerror=1;\
114 xtc1=0;\
115 xtcdelta=1E-4;\
116 if (abs(xtcerror) > xtcdelta) begin\
117     xtc1=xtc1+1;\
118     xtcx0=xtcx;\
119     fht(xtcVg,xtcVfb,xtcx0,xtcB,xtcalphasu,xtcBeta,
120         xtcepsilon,xtcVd,xtcphit,xtcerror);\
121     xtcx=xtcx0+xtcerror;\
122 end\
123 if (abs(xtcerror) > xtcdelta) begin\
124     xtc1=xtc1+1;\

```


(Continued.)

```

108   xtcx0=xtcx;\
109   'fht(xtcVg,xtcVfb,xtcx0,xtcB,xtcalphasu,xtcBeta,
      xtcepsilon,xtcVd,xtcphit,xtcerror);\
110   xtcx=xtcx0+xtcerror;\
111   end\
112   if (abs(xtcerror) > xtcdelta) begin\
113     xtc1=xtci+1;\
114     xtcx0=xtcx;\
115     'fht(xtcVg,xtcVfb,xtcx0,xtcB,xtcalphasu,xtcBeta,
          xtcepsilon,xtcVd,xtcphit,xtcerror);\
116     xtcx=xtcx0+xtcerror;\
117   end\
118   rxtc=xtcx;
119   /** Surface Potential **/
120   'define fps(psxtc,psphit,psVd,rps)\
121   rps=psxtc*psphit+psVd;
122   /** Difference of Potential ALPHA **/
123   'define falfa(alfaalphasu,alfaB,alfaxtc,ralfa)\
124   falfax1=alfaB*exp(alfaxtc);\
125   'flambert(falfax1,falfax2);\
126   ralfa=alfaalphasu+falfax2;
127   /** Minimum of Potential PHlmin **/
128   'define fdeltaphimin(dpmVgt,dpmVfb,dpmVd,dpmq,dpmNd,
      dpmEs,dpmlambdao,dpmVbis,dpmNdext,dpmL,
      rdeltaphimin)
129   dpmfiopf=dpmVgt-dpmVfb+(dpmq*dpmNd)/(dpmEs)
      *pow(dpmlambdao,2);\
130   oper1=1+((2*(dpmVbis-dpmfiopf))/((pow(dpmlambdao,2))*
      (dpmq*dpmNdext)/(dpmEs)));\
131   'ffsqrt(oper1,fdeltapx1);\
132   dpmdeltaVbis=dpmVbis-dpmfiopf+(pow(dpmlambdao,2)*
      (dpmq*dpmNdext)/(dpmEs)*(1-fdeltapx1));\
133   oper2=1+((2*(dpmVbis+dpmVd-dpmfiopf))/((pow(dpmlamb-
      dao,2)*(dpmq*dpmNdext)/(dpmEs)));\
134   'ffsqrt(oper2,fdeltapx2);\
135   dpmdeltaVbid=dpmVbis+dpmVd-dpmfiopf+(pow(dpmlamb-
      dao,2)*(dpmq*dpmNdext)/(dpmEs)*(1-fdeltapx2));\
136   dpmVbisef=dpmVbis-dpmdeltaVbis;\
137   dpmVbidef=dpmVbis+dpmVd-dpmdeltaVbid;\
138   dpmVbisf=dpmVbisef;\
139   dpmVbid=dpmVbidef;\
140   dpmUs=dpmVbisf-dpmfiopf;\
141   dpmUd=dpmVbid-dpmfiopf;\
142   'ffsqrt(-(dpmUs*dpmUs+dpmUd*dpmUd)+2*dpmUs*
      dpmUd*cosh(dpmL/dpmlambdao),fdeltapx3);\
143   rdeltaphimin=fdeltapx3/sinh(dpmL/dpmlambdao);
144   /** hypergeometric gaussian 2f1 function **/
145   'define fFint(b,z,x,rFint)\
146   fFintx1 = b-1;\
147   fFintx2 = 1-(z*x);\
148   rFint=pow(x,fFintx1)/(fFintx2);
149   /** hypergeometric gaussian 2f1 function with a=1, b=n
      +1, c=n+2, n=entero>=0 **/
150   'define fhypergeo(hya,hyb,hyc,hyz,rhyper)\
151   hyh=0.1;\
152   hytol1=5e-2;\
153   hytol2=1e-2;\
154   hyx=0;\
155   hyaux=0;\
156   while(hyx<1) begin\
157     if ((hyx+hyh)>1) begin\

```

(Continued.)

```

158     hyh=1-hyx;\
159     end\
160     'fFint(hyb,hyz,hyx,fhypergx1);\
161     'fFint(hyb,hyz,hyx+hyh,fhypergx2);\
162     hyquad1=hyh*0.5*(fhypergx1+fhypergx2);\
163     'fFint(hyb,hyz,hyx,fhypergx3);\
164     'fFint(hyb,hyz,hyx+hyh*0.5,fhypergx4);\
165     'fFint(hyb,hyz,hyx+hyh,fhypergx5);\
166     hyquad2=hyh/6*(fhypergx3+4*fhypergx4+fhy-
      pergx5);\
167     if(abs((hyquad1-hyquad2)>hytol1)) begin\
168       hyh=hyh . 0 . 5; \
169     end else begin\
170       hyaux=hyaux+hyquad2;\
171       hyx=hyx+hyh;\
172       if (abs((hyquad1-hyquad2)<hytol2)) begin\
173         hyh=2*hyh;\
174       end\
175     end\
176   end\
177   rhyper=hyb*hyaux;
178   /** SaN function **/
179   'define fSaN(z,SaN1)\
180   SaN1=-3.937e-4 + 0.01132*z + (0.3563*z*z)
      +(0.035*z*z*z) + (0.0027*z*z*z*z) +(8.9642e
      -5*z*z*z*z*z);
181   /** SaP function **/
182   'define fSaP(z,SaP1)\
183   SaP1=0.00118 - 0.00167*z + (0.349*z*z)
      +(0.04735*z*z*z) + (0.000565*z*z*z*z)
      +(0.00143*z*z*z*z*z);
184   /** TT function **/
185   'define fTT(z,x0,rTT)\
186   TTsigma2=0.08383;\
187   TTsigma3=0.00725;\
188   TTsigma4=2.57171e-4;\
189   fttvar=z/x0;\
190   'fhypergeo(1,3,4,fttvar,fTTx1);\
191   TTaux=TTsigma2*pow(z,3)*0.333*fTTx1;\
192   'fhypergeo(1,4,5,fttvar,fTTx2);\
193   TTaux=TTaux+TTsigma3*pow(z,3+1)*(0.25)*fTTx2;\
194   'fhypergeo(1,5,6,fttvar,fTTx3);\
195   TTaux=TTaux+TTsigma4*pow(z,4+1)*(0.2)*fTTx3;\
196   rTT=1/x0*TTaux;
197   /** Sb function **/
198   'define fSb(Sbz,Sbx0,rSb)\
199   Sbva=(Sbz-Sbx0);\
200   'fTT(Sbz,Sbx0,fSbx1);\
201   rSb=(0.01122*ln(Sbva)-(0.66782*(Sbz+Sbx0*ln(Sbva)))
      +(fSbx1);
202   /** Sbt funtion **/
203   'define fSbt(SbtVg,SbtVd,SbtVs,SbtVfb,SbtVt,Sbtalphasu,
      SbtB,SbtBeta,Sbtepsilon,Sbtphit,Sbtq,SbtNd,SbtEs,
      Sbtlambda0,Sbtx0,rSbt)\
204   fSbtaux1=SbtVt-0.2;\
205   'fxtc(fSbtaux1,SbtVs,SbtVfb,SbtVt,Sbtalphasu,SbtB,SbtBeta,
      Sbtepsilon,Sbtphit,Sbtq,SbtNd,SbtEs,Sbtlambda0,
      Sbtxtc02);\
206   'falfa(Sbtalphasu,SbtB,Sbtxtc02,Sbtalfa02);\
207   SbtA02=Sbtepsilon*Sbtalfa02;\
208   fSbtaux2=SbtVt-0.4;\

```

(Continued.)

```

209 `fxtc(fSbtaux2,SbtVs,SbtVfb,SbtVt,Sbtalphasu,SbtB,SbtBeta,
    Sbtepsilon,Sbtphit,Sbtq,SbtNd,SbtEs,Sbtlambda0,
    Sbtxtc04);`
210 `falfa(Sbtalphasu,SbtB,Sbtxtc04,Sbtalfa04);`
211 SbtA04=Sbtepsilon*Sbtalfa04;`
212 `fSb(SbtA02,SbtX0,fSbtaux3);`
213 `fSb(SbtA04,SbtX0,fSbtaux5);`
214 rSbt=fSbtaux3 + (fSbtaux3-fSbtaux5)*5 * (SbtVg - (SbtVt
    -0.2)-(SbtVd-SbtVs) );
215 /** Final Sb Solution called S3x **/
216 `define fS3x(S3xVg,S3xVd,S3xVs,S3xVfb,S3xVt,S3xalphasu,
    S3xB,S3xBeta,S3xepsilon,S3xphit,S3xq,S3xNd,S3xEs,
    S3xlambda0,S3xx0,rS3x)`
217 if (S3xVg<(S3xVt+S3xVd-0.25)) begin`
218     `fSbt(S3xVg,S3xVd,S3xVs,S3xVfb,S3xVt,S3xalphasu,
        S3xB,S3xBeta,S3xepsilon,S3xphit,S3xq,S3xNd,
        S3xEs,S3xlambda0,S3xx0,rS3x);`
219 end else begin`
220     `fxtc(S3xVg,S3xVd,S3xVfb,S3xVt,S3xalphasu,S3xB,
        S3xBeta,S3xepsilon,S3xphit,S3xq,S3xNd,S3xEs,
        S3xlambda0, S3xxt_c);`
221     `falfa(S3xalphasu,S3xB, S3xxt_c,S3xalfaC);`
222     fS3xifop=S3xepsilon*S3xalfaC;`
223     `fSb(fS3xifop,S3xx0,rS3x);`
224 end
225 /** Subx Function **/
226 `define fSubx(x,x0,rSubx)`
227 `ffsqrt((-1-x),fSubxvar1);`
228 `ffsqrt((abs(1+x0),fSubxvar2);`
229 rSubx= -2*(fSubxvar1-fSubxvar2*atan(fSubxvar1/
    fSubxvar2));
230
231 /** *****
232 ***** Verilog-A Module and Parameters *****
233 /** *****
234
235 module DJLT (d, g, s);
236
237 inout d, g, s;
238 electrical d,g,s;
239
240 parameter real Npoly = 1E20 from [0.0:inf];
241 parameter real L = 1000E-7 from [0.0:inf];
242 parameter real ts = 10E-7 from [0.0:inf];
243 parameter real Nss = 5E10 from [0.0:inf];
244 parameter real Hfin = 1E-4 from [0.0:inf];
245 parameter real Ndext = 1E20 from [0.0:inf];
246 parameter real Lext = 30E-7 from [0.0:inf];
247 parameter real WW = 1E-4 from [0.0:inf];
248 parameter real Nd = 1e19 from [0.0:inf];
249 parameter real P1 = -0.015 from [-inf:inf];
250 parameter real uo = 100 from [0.0:inf];
251 parameter real R = 216 from [0.0:inf];
252 parameter real n = 0.3 from [0.0:inf];
253 parameter real theta1 = -0.02 from [-inf:inf];
254 parameter real theta2 = 0.02 from (-inf:inf);
255 parameter real vsat = 1E7 from [0.0:inf];
256 parameter real lambda = 0 from [0.0:inf];
257 parameter real Eta = 0.15 from (0.0:inf);
258 parameter real phimet = 5.198 from (0.0:inf);
259 parameter real to = 2E-7 from [0.0:inf];

```

(Continued.)

```

260 parameter real Va = 0.75 from [0.0:inf];
261
262 /** *****
263 real alpha1,ft,alpha1,ft1,alpha2,ft2,alpha3,ft3,fl1,tmpl,flamx1;
264 real c11,c21,fl21,w11,dwl,xtcVx1,xtcVx2,xtcalphaapprox,
    xtcsaprox;
265 real xtcfiop,xtcxsub1,xtcxsub2,xtcxar,xtcxT,xtcxF,xtcerror,
    xtcx0;
266 real xtcdelta,xtcx,xtci,htxm,dpmfiop,dpmdeltaVbis,
    dpmdeltaVbid;
267 real dpmVbisef,dpmVbidef,dpmVbisf,dpmVbid,dpmUs,
    dpmUd;
268 real hyh,hytol1,hytol2,hyx,hyaux,hyquad1,hyquad2;
269 real Sbtxtc02,Sbtxtc04,Sbtalfa02,Sbtalfa04,SbtA02,SbtA04;
270 real TTaux,TTsigma2,TTsigma3,TTsigma4;
271 real S3xxt_c,S3xalfaC,Sbva,fS3xifop,ftvar;
272 real Eox,kBe,Es,phit,Eg,Ego,DEg,phiEg,Egp,Egop,DEgp,
    phiEg,Eip,Ef;
273 real Nc,Nv,ni,ai,niep,phifp,Efp,Ei,phiip,phifext,phif,phii;
274 real Co,Cs,Qb,qb,Qo,qef,phisem,phimsM,phimsP;
275 real phims,Vfb,delta,gamma,tn,tnA,P0;
276 real phidsu,alphasu,alphasul,B,Beta,epsilon,alpat,Vt;
277 real lambda0,fiop,alphaapprox,psaprox;
278 real Vx1,Vx2;
279 real xt_c,psC,alphaC,poC;
280 real q1a,q1b,q1am,q1bm,q2,q2m,q1,q1m,qt,qtM;
281 real Vbis, deltaphiminv, deltaphimini,Vgef,Vsat0,Vsat1,Vgtrans;
282 real var1,Vdsat,Vdef,Vdefs;
283 real us,uef,deltaL,VL,Ko,F,FF,KK;
284 real equis0,alphaapproxS,psaproxS;
285 real xt_c,psCS,alphaCS,poCS,q1aS,q1bS,q1amS,q1bmS;
286 real q2S,q2mS,q1S,q1mS,qtS,qtM;
287 real IA;
288 real S3xs, S3xD;
289 real D0x,D11x,D12x,D13x,D14x,D1subx,D1atx,D1x;
290 real S22xD, S22xS,D2x,Dx,D22x;
291 real ffsqrt1,ffsqrt2,ffsqrt3,ffsqrt4,ffsqrt5,ffsqrt6,ffsqrt7,ffsqrt8;
292 real fsgn1,fsgn2,fsgn3,fsgn4,fsgn5,fsgn6,ffsqrt9;
293 real fSaN1,fSaN2;
294 real fSubx1,fSubx2;
295 real SaPaux1,SaPaux2;
296 real fhxt1,fhxt2,fhxt3,fhxt4,fhxt5,fhxt6,fhxt7,fhxt8,fhxt9,
    fhxt10;
297 real fxtcx1,fxtcx2,fhxt11,fhxt12,fhxt13,fhxt14,fhxt15,fhxt16,
    fhxt17;
298 real falfax1,falfax2;
299 real fdeltapx1,fdeltapx2,fdeltapx3;
300 real fhypergx1,fhypergx2,fhypergx3,fhypergx4,fhypergx5;
301 real fTTx1,fTTx2,fTTx3;
302 real fSbx1,fSbtaux1,fSbtaux2,fSbtaux3,fSbtaux5;
303 real fSubxvar1,fSubxvar2,oper1,oper2;
304 real fFintx1,fFintx2,lamb1,aux1,aux2;
305
306 /** *****
307 ***** Behavioral Description *****
308 /** *****
309 analog begin
310     Eox='Eo*'ko;
311     kBe='kB/'q;
312     Es='Eo*'ks;
313     phit=('kB*'T)/q;

```

(Continued.)

```

314 /** Bandgap **/
315   'ffsqr((pow(ln(Nd/(1E17)),2)+0.5),Vx1);
316   DEg=(9E-3)*(ln(Nd/(1E17))+Vx1);
317   Ego=1.08+(4.73E-4)*(pow(300,2)/(300+636))-
      (pow('T,2)/('T+636));
318   Eg=Ego-DEg;
319   phiEg=-Eg;
320   'ffsqr((pow(ln(Npoly/(1E17)),2)+0.5),Vx1);
321   DEgp=(9E-3)*(ln(Npoly/(1E17))+Vx1);
322   Egop=1.08+(4.73E-4)*(pow(300,2)/(300+636))-
      (pow('T,2)/('T+636));
323   Egp=Egop-DEgp;
324   phiEgp=-Egp;
325 /**Density of States **/
326   Nc=2.8E19*pow('T/300,1.5);
327   Nv=1.04E19*pow('T/300,1.5);
328   'ffsqr(Nc*Nv,Vx1);
329 /**Intrinsic Concentration **/
330   ni=Vx1*exp(-(Eg)/(2*phit));
331   ai=ln(ni);
332   niep=Vx1*exp(-(Egp)/(2*phit));
333 /** Fermi Level in the Silicon **/
334   phif=-phit*ln(Nd/ni);
335   Ef=-phif;
336 /** Fermi Level in Poly **/
337   phifp=phit*ln(Npoly/niep);
338   Efp=-phifp;
339 /** Intrinsic Level **/
340   Ei=0.5*Eg+(0.5*phit*ln(Nv/Nc));
341   phii=-Ei;
342   Eip=0.5*Egp+(0.5*phit*ln(Nv/Nc));
343   phiip=-Eip;
344 /** Fermi Level in Extensions **/
345   phifext=-phit*ln(Ndext/ni);
346 /** Capacitances **/
347   Co=Eox/to;
348   Cs=Es/ts;
349 /** Ion Concentrations **/
350   Qb='q*Nd*ts;
351   qb=Qb/(Co*phit);
352 /** Charging Interface **/
353   Qo='q*Nss;
354 /** Extractive Work **/
355   xef=4.17+DEg*0.5;
356   phisem=xef+Eg*0.5+phif;
357   phimsM=phimet-phisem;
358   phimsP=phit*ln((Npoly*Nd)/(ni*niep));
359 /** Flat Band Voltage **/
360   phims=phimsM;
361   Vfb=phims-(Qo/Co);
362 /** Auxiliary Relationships **/
363   delta=Cs/(Co+Cs);
364   gamma=Co/(4*Cs);
365   'ffsqr((Es/(2*Eox)*to*ts),tn);
366   'ffsqr(2,Vx1);
367   'ffsqr((1+(4*Cs/Co)),Vx2);
368   tnA=ts/(2*Vx1)*Vx2;
369   P0=phit;
370 /** Difference of Potentials in Deep Subthreshold **/
371   phidsu=-Qb/(8*Cs);
372   alphasu=phidsu/phit;

```

(Continued.)

```

373   alphasul=-'q*Nd*(pow(ts,2))/(8*Es*phit);
374   B=-alphasu*exp(-alphasu);
375   'ffsqr((qb/(2*gamma)),Beta);
376   epsilon=1-(1/alphasu);
377   equis0=epsilon*alphasu;
378 /** Threshold Voltage **/
379   alphasul=alphasu/(1-alphasu)*(1-alphasu*pow
      ((1-1/(2*qb)),2));
380   Vt=Vfb-phit*(qb/2-0.25-alphasul-ln(1-alphasul/alphasu));
381 /** Natural Length Double Gate **/
382   'ffsqr((Es/(2*Eox)*(1+(Eox*ts)/(4*Es*to))*ts*to),
      lambdao);
383   Vbis=Va+phif;
384 /** Potential Barrier Change Described by Phimin **/
385   if (V(g) < Vt) begin
386     'fdeltaphimin(V(g),Vfb,V(d),'q,Nd,Es,lambdao,Vbis,Ndext,
      L, delta_phi_min_v);
387   end else begin
388     'fdeltaphimin(Vt,Vfb,V(d),'q,Nd,Es,lambdao,Vbis,
      Ndext,
      L, delta_phi_min_v);
389   end
390   'fdeltaphimin(Vt,Vfb,V(d),'q,Nd,Es,lambdao,Vbis,
      Ndext,
      L, delta_phi_min_t);
391 /** Effective Voltage VGS **/
392   aux1=delta_phi_min_v+V(g)*(0.5*(1-tanh(50*(V
      (g)-Vt)));
393   aux2=delta_phi_min_t+V(g)*(0.5*(1+tanh(50*(V
      (g)-Vt)));
394   Vgef=aux1+aux2;
395 /** Saturation Voltage **/
396   Vsat0=Vgef-Vt;
397   Vsat1=0.08+Eta*(pow(L*vsat,0.33))*(Vgef-Vt);
398 /** Transition between Vdsat **/
399   Vgtrans=((0.08)/(1-Eta*(pow(L*vsat,0.33)))+Vt);
400 /** Saturation Voltage **/
401   var1=Eta*(pow(L*vsat,0.33));
402   if (var1 >= 1) begin
403     Vdsat=Vsat1*(0.5)*(1-tanh(2*(Vgef-Vgtrans)))
      +Vsat0*(0.5)*(1+tanh(2*(Vgef-Vgtrans)));
404   end else begin
405     Vdsat=Vsat0*(0.5)*(1-tanh(2*(Vgef-Vgtrans)))
      +Vsat1*(0.5)*(1+tanh(2*(Vgef-Vgtrans)));
406   end
407   if (L >= 200) begin
408     Vdsat=Vsat0;
409   end
410 /** Effective Saturation Voltage **/
411   'ffsqr((pow((V(d)-Vdsat+P0),2))+(4*Vdsat*P0),
      ffsqr1);
412   Vdef=Vdsat+(0.5*(V(d)-Vdsat+P0-ffsqr1));
413 /** Effective Drain Voltage **/
414   Vdefs=(V(d)*0.5*(1-tanh((Vgef-Vt)*15)))+(Vdef*0.5*(1
      +tanh((Vgef-Vt)*15)));
415 /** Potential at the Center **/
416   fiop=Vgef-Vfb+('q*Nd)/(Es)*pow(lambdao,2);
417 /** Difference of Potentials **/
418   alphaapprox=alphasu*(1-exp((fiop-Vdefs)/phit));
419   alphaapproxS=alphasu*(1-exp((fiop-V(s))/phit));
420 /** Surface Potential **/

```

(Continued.)

```

421 psaprox=alphaaprox*phit+fiop;
422 psaproxS=alphaaproxS*phit+fiop;
423 /** Calculated Surface Potential **/
424 'fxtc(Vgef,Vdefs,Vfb,Vt,alphasu,B,Beta,epsilon,phit,'q,Nd,
    Es,
        lambdao, xt_c);
425 'fps(xt_c,phit,Vdefs,psC);
426 /** Calculated Difference of Potentials **/
427 'falfa(alphasu,B, xt_c,alphaC);
428 /** Potential Calculated at the Center **/
429 poC=psC-phit*alphaC;
430 'fxtc(Vgef,V(s),Vfb,Vt,alphasu,B,Beta,epsilon,phit,'q,Nd,
    Es,lambdao, xt_cS);
431 'fps(xt_cS,phit,V(s),psCS);
432 'falfa(alphasu,B, xt_cS,alphaCS);
433 poCS=psCS-phit*alphaCS;
434 /** Mobile Charges **/
435 'ffsqt(exp(epsilon*alphaC)-(epsilon*alphaC)-1,ffsqt2);
436 'fsgn(alphaC,fsgn1);
437 q1a=-(fsgn1*Beta)*ffsqt2;
438 'ffsqt(exp(epsilon*alphaCS)-(epsilon*alphaCS)-1,
    ffsqt3);
439 'fsgn(alphaCS,fsgn2);
440 q1aS=-(fsgn2*Beta)*ffsqt3;
441 'ffsqt(abs((-1*(epsilon*alphaC))-1),ffsqt4);
442 'fsgn(alphaC,fsgn3);
443 q1b=-(fsgn3*Beta)*ffsqt4;
444 'ffsqt(abs((-1*(epsilon*alphaCS))-1),ffsqt5);
445 'fsgn(alphaCS,fsgn4);
446 q1bS=-(fsgn4*Beta)*ffsqt5;
447 q1am=q1a-qb/2;
448 q1bm=q1b-qb/2;
449 q1amS=q1aS-qb/2;
450 q1bmS=q1bS-qb/2;
451 'ffsqt(exp(xt_c)-xt_c-1,ffsqt6);
452 'fsgn(alphaC,fsgn5);
453 q2=-(fsgn5*Beta)*ffsqt6;
454 'ffsqt(exp(xt_cS)-xt_cS-1,ffsqt7);
455 'fsgn(alphaCS,fsgn6);
456 q2S=-(fsgn6*Beta)*ffsqt7;
457 q2m=q2-qb*0.5;
458 q2mS=q2S-qb*0.5;
459 q1=(q1b*0.5)*(1-tanh((Vgef-(Vt+Vdefs))*20))
    +(q1a*0.5)*(1+tanh((Vgef-(Vt+Vdefs))*20));
460 q1S=(q1bS*0.5)*(1-tanh((Vgef-(Vt+V(s))*20))
    +(q1aS*0.5)*(1
        +tanh((Vgef-(Vt+V(s))*20)));
461 q1m=q1-qb*0.5;
462 q1mS=q1S-qb*0.5;
463 qt=(q1*0.5)*(1-tanh((Vgef-(Vfb+Vdefs))*20))+(q2*0.5)*
    (1
        +tanh((Vgef-(Vfb+Vdefs))*20));
464 qtS=(q1S*0.5)*(1-tanh((Vgef-(Vfb+V(s))*20)))+(q2S*0.5)
    *
        (1+tanh((Vgef-(Vfb+V(s))*20));
465 qtm=qt-qb*0.5;

```

(Continued.)

```

466 qtmS=qtS-qb*0.5;
467 /** Mobility **/
468 us=uo/(1+((theta1*(Vgef-Vfb)+theta2*Vdef)*1/2*(1
    +tanh
        (5*(Vgef-Vfb)))));
469 'ffsqt(1+(pow(((us*Vdef)/(L*vsat)),2)),ffsqt8);
470 uef=us/ffsqt8;
471 /** shortening channel **/
472 'ffsqt(((2*Es)/('q*Nd))*(V(d)-Vdefs),ffsqt9);
473 deltaL=lambda*ffsqt9;
474 VL=1/(1-(deltaL/L));
475 /** Series resistance **/
476 Ko=2*WW/L*Co;
477 F=uef/(1+(R*Ko*uef)*(Vgef-Vt-n*Vdefs)*0.5*(1+tanh
    (2*(Vgef-Vt-n*Vdefs)))));
478 FF=F*VL;
479 KK=Ko*phit*FF;
480 /** Drain Current **/
481 /** Drain Current in Depletion Regime **/
482 D0x=qb/2*(Vdefs-V(s));
483 D11x=(phit/2)*(qtS*qtS-qt*qt);
484 'fSaN(epsilon*alphaCS,fSaN1);
485 'fSaN(epsilon*alphaC,fSaN2);
486 D12x=(phit*(Beta/epsilon))* (fSaN1 - fSaN2);
487 'fS3x(Vgef,Vdefs,V(s),Vfb,Vt,alphasu,B,Beta,epsilon,
    phit,'q,
        Nd,Es,lambdao,equis0, S3x_D);
488 'fS3x(Vgef,V(s),V(s),Vfb,Vt,alphasu,B,Beta,epsilon,phit,'q,
    Nd,
        Es,lambdao,equis0, S3x_S);
489 D13x=(-(phit*Beta)* (S3x_S-S3x_D))+((V(d)
    *0.013)+0.01);
490 'fSubx(epsilon*alphaCS,equis0,fSubx1);
491 'fSubx(epsilon*alphaC,equis0,fSubx2);
492 D14x=Beta*phit*(fSubx1 - fSubx2);
493 D1subx=-1*(D11x+D12x)*0.034;
494 D1atx=D0x+(P1*(1.1e-4-Vdefs))+D11x+D12x+D13x;
495 D1x=(D1subx*0.5*(1-tanh(55*(Vgef-Vt))))+(D1atx*0.5*(1
    +tanh(55*(Vgef-Vt)))));
496 /** Drain Current in Accumulation Regime **/
497 SaPaux1=(Vgef-Vfb-Vdefs)/phit + qt;
498 'fSaP(SaPaux1, S22x_D);
499 SaPaux2=(Vgef-Vfb-V(s))/phit + qtS;
500 'fSaP(SaPaux2, S22x_S);
501 D22x=phit*Beta*(S22x_S- S22x_D);
502 D2x=D0x + D11x + phit*Beta*(S22x_S-S22x_D);
503 /** General Solution in Both Regions **/
504 Dx=D1x*0.5*(1-tanh(20*(Vgef-(Vfb+Vdefs)))) +
    D2x*0.5*(1
        +tanh(20*(Vgef-(Vfb+Vdefs)))));
505 IA=KK*Dx;
506 I(d) <+ IA;
507 end
508 endmodule

```

References

- [1] Colinge J P et al 2009 SOI gated resistor: CMOS without junctions *IEEE Int. SOI Conf.* pp 1–2
- [2] Chen C-Yu, Lin J-T and Chiang M-H 2013 Comparative study of process variations in junctionless and conventional double-gate MOSFETs *IEEE 8th Nanotechnology Materials and Devices Conf. (NMDC)* pp 81–3
- [3] Gnani E, Gnudi A, Reggiani S and Baccarani G 2011 Theory of the junctionless nanowire fet *IEEE Trans. Electron Devices*, **58** 2903–10
- [4] Han M-H, Chang C-Y, Chen H-B, Wu J-J, Ya-C Cheng and Wu Y-C 2013 Performance comparison between bulk and soi junctionless transistors *IEEE Electron Device Lett.* **34** 169–71
- [5] Jeon D-Y, Park So J, Mouis M, Barraud S, Kim G-T and Ghibaudo G 2013 Effects of channel width variation on electrical characteristics of tri-gate junctionless transistors *Solid-State Electron.* **81** 58–62
- [6] Mariniello G, Cerdeira A, Estrada M, Doria R T, Trevisoli R D, de Souza M and Pavanello M A 2013 Analysis of charges densities in multiple-gates SOI nMOS junctionless *Symp. Microelectronics Technology and Devices (SBMicro)* pp 1–4
- [7] Holtij T, Schwarz M, Graef M, Hain F, Kloes A and Iniguez B 2013 Model for investigation of ion/ioff ratios in short-channel junctionless double gate mosfets *14th Int. Conf. Ultimate Integration on Silicon (ULIS)* pp 85–8
- [8] Hu G, Xiang P, Ding Z, Liu R, Wang L and Tang T-Ao 2014 Analytical models for electric potential, threshold voltage, and subthreshold swing of junctionless surrounding-gate transistors *IEEE Trans. Electron Devices* **61** 688–95
- [9] Joo M-K, Mouis M, Jeon D-Y, Barraud S, Park So J, Kim G-T and Ghibaudo G 2014 Flat-band voltage and low-field mobility analysis of junctionless transistors under low-temperature *Semicond. Sci. Technol.* **29** 045024
- [10] Woo J-Ho, Choi Ji-M and Choi Y-K 2013 Analytical threshold voltage model of junctionless double-gate mosfets with localized charges *IEEE Trans. Electron Devices* **60** 2951–5
- [11] Duarte J P, Choi S-J, Moon D-II and Choi Y-K 2011 Simple analytical bulk current model for long-channel double-gate junctionless transistors *IEEE Electron Device Lett.* **32** 704–6
- [12] Sallese J-M, Chevillon N, Lallement C, Iniguez B and Prgaldiny F 2011 Charge-based modeling of junctionless double-gate field-effect transistors *IEEE Trans. Electron Devices* **58** 2628–37
- [13] Trevisoli R D, Doria R T, de Souza M, Das S, Ferain I and Pavanello M A 2012 Surface-potential-based drain current analytical model for triple-gate junctionless nanowire transistors *IEEE Trans. Electron Devices* **59** 3510–8
- [14] Holtij T, Graef M, Hain F M, Kloes A and Iniguez B 2014 Compact model for short-channel junctionless accumulation mode double gate mosfets *IEEE Trans. Electron Devices* **61** 288–99
- [15] Lime F, Santana E and Iniguez B 2013 A simple compact model for long-channel junctionless double gate MOSFETs *Solid-State Electron.* **80** 28–32
- [16] Sallese J-M, Jazaeri F, Barbut L, Chevillon N and Lallement C 2013 A common core model for junctionless nanowires and symmetric double-gate fets *IEEE Trans. Electron Devices* **60** 4277–80
- [17] Yesayan A, Prgaldiny F and Sallese J-M 2013 Explicit drain current model of junctionless double-gate field-effect transistors *Solid-State Electron.* **89** 134–8
- [18] Ávila-Herrera F, Cerdeira A, Paz B C, Estrada M, Iniguez B and Pavanello M A 2015 Compact model for short-channel symmetric double-gate junctionless transistors *Solid-State Electron.* **111** 196–203
- [19] Cerdeira A, Estrada M, Iniguez B, Trevisoli R D, Doria R T, de Souza M and Pavanello M A 2013 Charge-based continuous model for long-channel symmetric double-gate junctionless transistors *Solid-State Electron.* **85** 59–63
- [20] Silvaco int. atlas. 2014
- [21] Cerdeira A, Ávila F, Iniguez B, de Souza M, Pavanello M A and Estrada M 2014 Compact core model for symmetric double-gate junctionless transistors *Solid-State Electron.* **94** 91–7
- [22] <http://ngspice.sourceforge.net/admshowto.html>